TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

1,048,576-WORD × 16-BIT FAST PAGE DYNAMIC RAM

DESCRIPTION

The TC5118160CJ/CFT is a fast page dynamic RAM organized as 1,048,576 words by 16 bits. The TC5118160CJ/CFT utilizes TOSHIBA's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. Multiplexed address inputs permit the TC5118160CJ/CFT to be packaged in a 42-pin plastic SOJ or a 50-pin plastic TSOP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. Other features include a single power supply of 5 V ± 10% tolerance and direct interfacing with high performance logic families such as Schottky TTL.

FEATURES

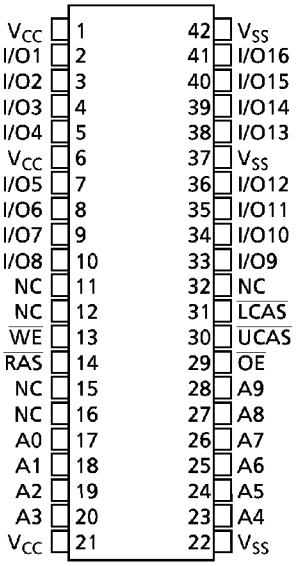
- 1,048,576-word by 16-bit organization
- Fast access time and cycle time

		TC5118160CJ/CFT	
		-50	-60
t_{RAC}	$\overline{RAS}$ Access Time	50 ns	60 ns
t_{AA}	Column Address Access Time	25 ns	30 ns
t_{CAC}	$\overline{CAS}$ Access Time	13 ns	15 ns
t_{RC}	Cycle Time	90 ns	110 ns
t_{PC}	Fast Page Mode Cycle Time	35 ns	40 ns

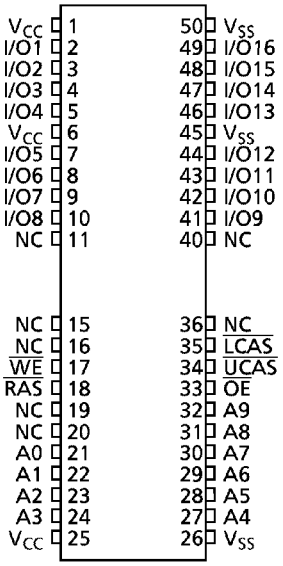
- Single power supply of 5 V ± 10% with a built-in V_{BB} generator
- Low-power dissipation (max)
  - Operating: 1237 mW (50 ns type)
  - : 1018 mW (60 ns type)
  - Stand by : 5.5 mW (both devices)
- Unlatched outputs at cycle end allows two-dimensional chip selection
- Read-Modify-Write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-Only refresh, Hidden refresh and Fast Page mode capability
- All inputs and outputs TTL-compatible
- 1024 refresh cycles per 16 ms
- Package
  - CJ : SOJ42-P-400-1.27, 1.66 grams
  - CFT: TSOP II 50/44-P-400-0.80, 0.53 grams

PIN ASSIGNMENT (TOP VIEW)

Plastic SOJ



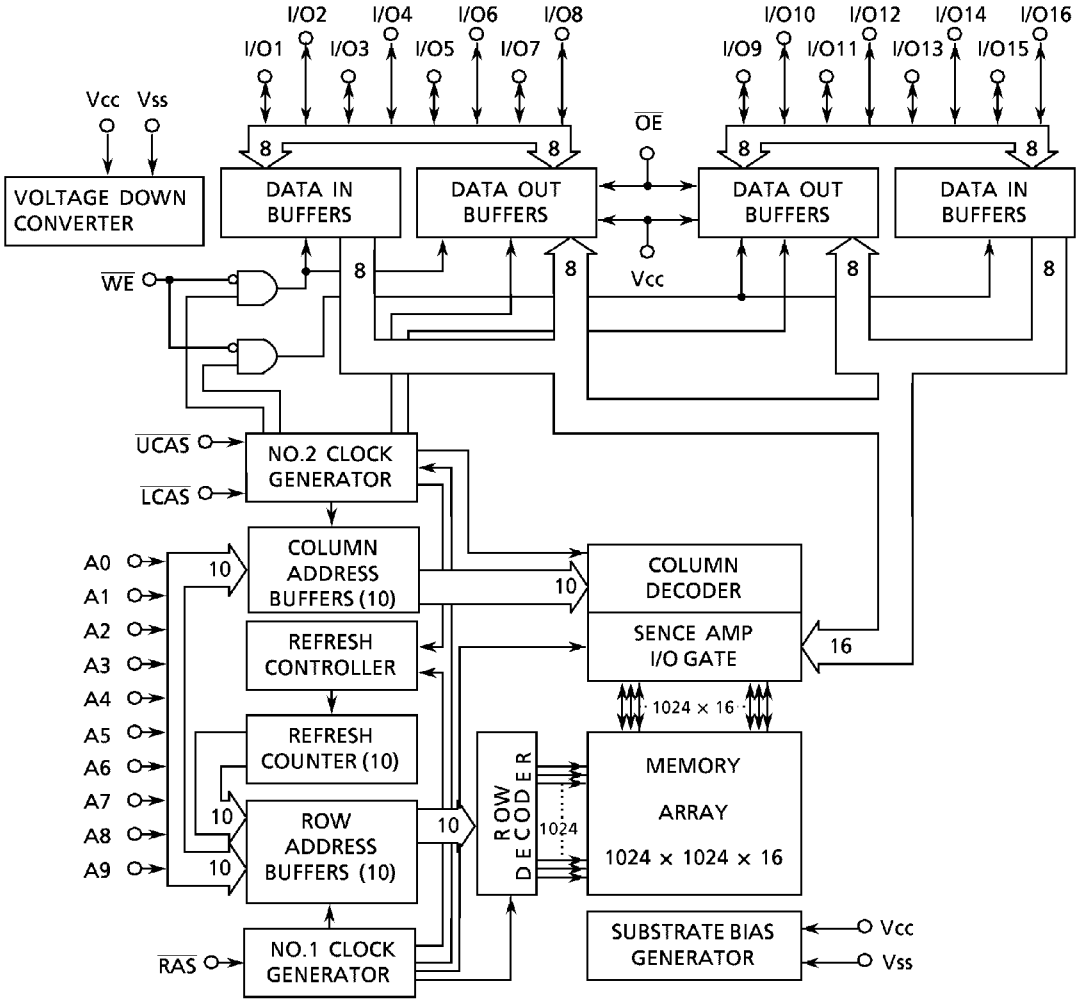
Plastic TSOP



PIN NAMES

A0 to A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe /Upper Byte Control
$\overline{LCAS}$	Column Address Strobe /Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O1 to I/O16	Data Input/Output
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
N.C.	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT	NOTES
Input Voltage	V_{IN}	− 0.5 to Vcc + 0.5	V	1
Output Voltage	V_{OUT}	− 0.5 to Vcc + 0.5	V	1
Power Supply Voltage	V_{CC}	− 0.5 to 7	V	1
Operating Temperature	T_{OPR}	0 to 70	°C	1
Storage Temperature	T_{STG}	− 55 to 150	°C	1
Soldering Temperature (10 s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1.6	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	V_{CC} + 0.5*	V	2
V_{IL}	Input Low Voltage	− 0.5**	−	0.8	V	2

* Vcc + 2.0 V at pulse width ≦ 20 ns. (pulse width is measured at Vcc)

** − 2.0 V at pulse width ≦ 20 ns. (pulse width is measured at Vss)

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, Ta = 0° to 70°C)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTES
I_{CC1}	OPERATING CURRENT Average Power Supply Operating Current ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: t_{RC} = t_{RC} min)	TC5118160CJ/CFT-50	–	225	mA	3, 4, 5
		TC5118160CJ/CFT-60	–	185		
I_{CC2}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH})		–	2	mA	
I_{CC3}	$\overline{RAS}$-ONLY REFRESH CURRENT Average Power Supply Current, $\overline{RAS}$-Only Mode ($\overline{RAS}$ Cycling, $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}: t_{RC} = t_{RC} min)	TC5118160CJ/CFT-50	–	225	mA	3, 5
		TC5118160CJ/CFT-60	–	185		
I_{CC4}	FAST PAGE MODE CURRENT Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling: t_{PC} = t_{PC} min)	TC5118160CJ/CFT-50	–	100	mA	3, 4, 5
		TC5118160CJ/CFT-60	–	90		
I_{CC5}	STANDBY CURRENT Power Supply Standby Current ($\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{CC} – 0.2 V)		–	1	mA	
I_{CC6}	$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CURRENT Average Power Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Cycling: t_{RC} = t_{RC} min)	TC5118160CJ/CFT-50	–	225	mA	3, 5
		TC5118160CJ/CFT-60	–	185		
$I_{I\ (L)}$	INPUT LEAKAGE CURRENT Input Leakage Current, any input (0 V ≦ V_{IN} ≦ V_{CC}, All Other Pins Not under Test = 0 V)		– 10	10	μA	
$I_{O\ (L)}$	OUTPUT LEAKAGE CURRENT (D_{OUT} Is disabled, 0 V ≦ V_{OUT} ≦ V_{CC})		– 10	10	μA	
V_{OH}	OUTPUT LEVEL Output H Level Voltage (I_{OUT} = – 5 mA)		2.4	–	V	
V_{OL}	OUTPUT LEVEL Output L Level Voltage (I_{OUT} = 4.2 mA)		–	0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5 V ± 10%, Ta = 0° to 70°C) (Notes 6, 7, 8)

SYMBOL	PARAMETER	TC5118160CJ/CFT				UNIT	NOTES
		-50		-60			
		MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	90	–	110	–	ns	
t_{RMW}	Read-Modify-Write Cycle Time	126	–	150	–	ns	
t_{PC}	Fast Page Mode Cycle Time	35	–	40	–	ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	71	–	80	–	ns	
t_{RAC}	Access Time from $\overline{RAS}$	–	50	–	60	ns	9,14,15
t_{CAC}	Access Time from $\overline{CAS}$	–	13	–	15	ns	9,14
t_{AA}	Access Time from Column Address	–	25	–	30	ns	9,15
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	30	–	35	ns	9
t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	13	0	15	ns	10
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	8
t_{RP}	$\overline{RAS}$ Precharge Time	30	–	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10,000	60	10,000	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	50	100,000	60	100,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	13	–	15	–	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge (Fast Page Mode)	30	–	35	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	50	–	60	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	13	10,000	15	10,000	ns	
t_{RCD}	$\overline{RAS}$-to-$\overline{CAS}$ Delay Time	18	37	20	45	ns	14
t_{RAD}	$\overline{RAS}$-to-Column-Address Delay Time	13	25	15	30	ns	15
t_{CRP}	$\overline{CAS}$-to-$\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	
t_{ASR}	Row Address Set up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	8	–	10	–	ns	
t_{ASC}	Column Address Set up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	8	–	10	–	ns	
t_{RAL}	Column-Address-to-$\overline{RAS}$ Lead Time	25	–	30	–	ns	
t_{RCS}	Read Command Set up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	11
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	ns	11

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL	PARAMETER	TC5118160CJ/CFT				UNIT	NOTES
		-50		-60			
		MIN	MAX	MIN	MAX		
t_{WCH}	Write Command Hold Time	8	–	10	–	ns	
t_{WP}	Write Command Pulse Width	8	–	10	–	ns	
t_{RWL}	Write-Command-to-$\overline{RAS}$ Lead Time	8	–	10	–	ns	
t_{CWL}	Write-Command-to-$\overline{CAS}$ Lead Time	8	–	10	–	ns	
t_{DS}	Data Set up Time	0	–	0	–	ns	12
t_{DH}	Data Hold Time	8	–	10	–	ns	12
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set up Time	0	–	0	–	ns	13
t_{CWD}	$\overline{CAS}$-to-$\overline{WE}$ Delay Time	36	–	40	–	ns	13
t_{RWD}	$\overline{RAS}$-to-$\overline{WE}$ Delay Time	73	–	85	–	ns	13
t_{AWD}	Column-Address-to-$\overline{WE}$ Delay Time	48	–	55	–	ns	13
t_{CPWD}	$\overline{CAS}$-Precharge-to-$\overline{WE}$ Delay Time	53	–	60	–	ns	13
t_{CSR}	$\overline{CAS}$ Set up Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	5	–	5	–	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Cycle)	8	–	10	–	ns	
t_{RPC}	$\overline{RAS}$-to-$\overline{CAS}$ Precharge Time	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle)	20	–	20	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	8	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	13	–	15	ns	9
t_{OED}	$\overline{OE}$-to-Data Delay	13	–	15	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	ns	
t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	13	0	15	ns	10
t_{OEH}	$\overline{OE}$ Command Hold Time	8	–	10	–	ns	
t_{ODS}	Output Disable Set up Time	0	–	0	–	ns	

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, Ta = 0° to 70°C)

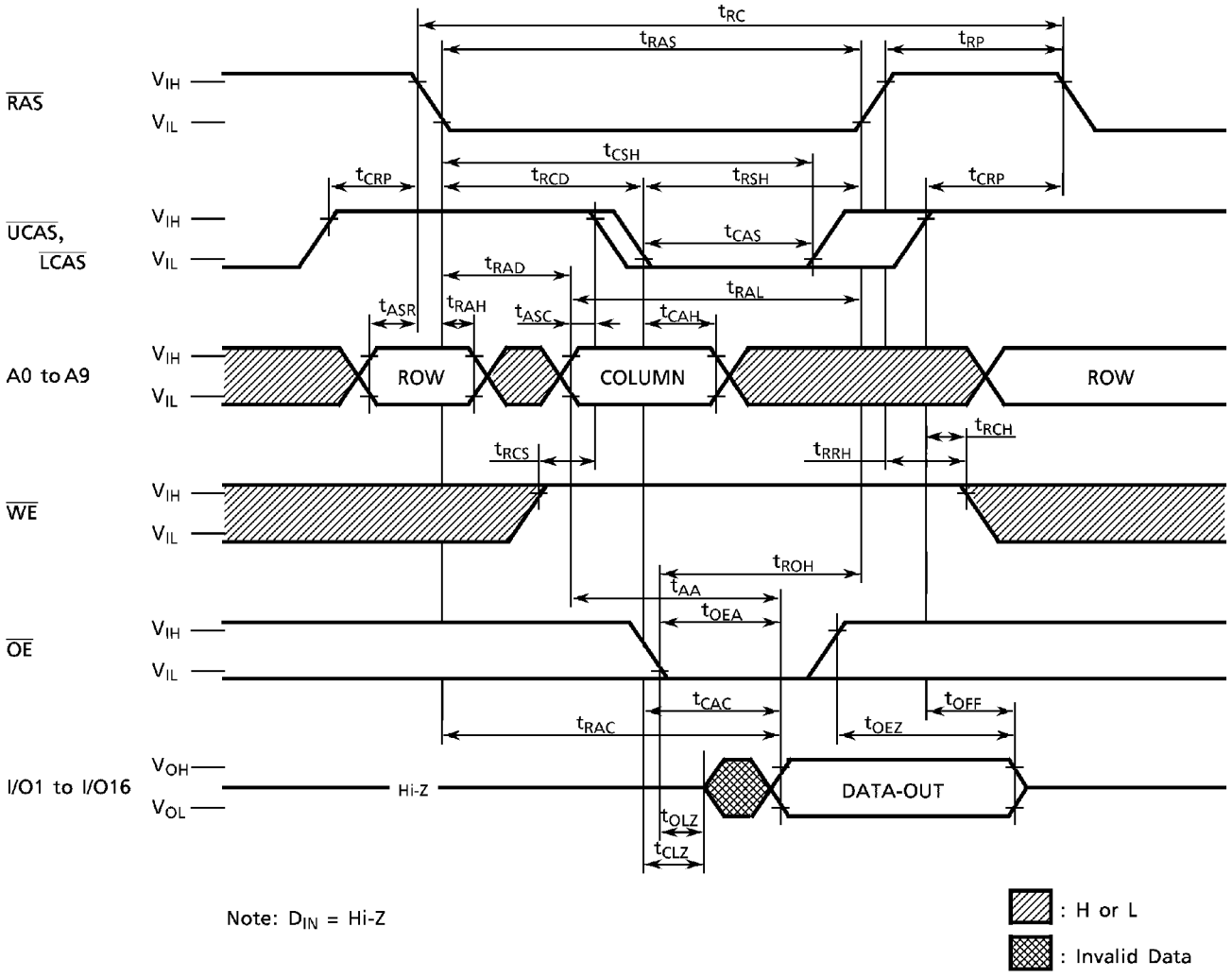
SYMBOL	PARAMETER	MIN	MAX	UNIT
C_{I1}	Input Capacitance (A0 to A9)	–	5	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_O	I/O Capacitance (I/O1 to I/O16)	–	7	pF

NOTES:

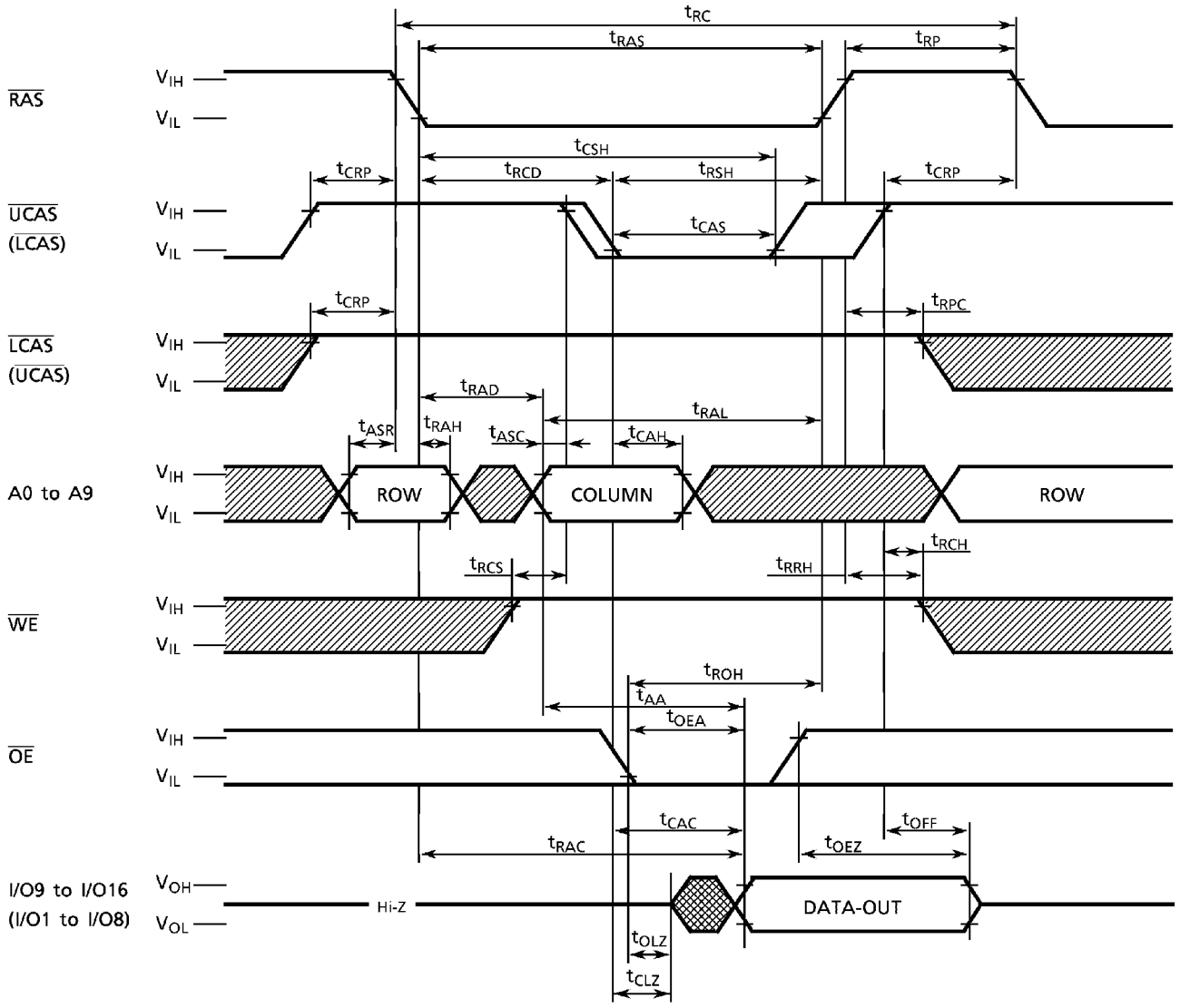
1. Conditions outside the limits listed under "Absolute Maximum Rating" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
4. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
5. Address can be changed once at most while $\overline{RAS}$ = V_{IL}. In case of I_{CC4}, it can be changed once at most during a Fast Page mode cycle (t_{PC}).
6. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$-Only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$-Only refresh cycles are required.
7. AC measurements assume t_T = 5 ns.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
9. This is measured with a load equivalent to 2 TTL loads and 100 pF.
10. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output goes open circuit and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
12. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge of $\overline{CAS}$ in Early Write cycles and to leading edge of $\overline{WE}$ in Read-Modify-Write cycles.
13. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an Early Write cycle and the data out pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geqq t_{RWD}$ (min), $t_{CWD} \geqq t_{CWD}$ (min), $t_{AWD} \geqq t_{AWD}$ (min) and $t_{CPWD} \geqq t_{CPWD}$ (min) (Fast Page mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met.
    t_{RCD} (max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is determined by t_{CAC}.
15. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met.
    t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is determined by t_{AA}.

TIMING DIAGRAMS

READ CYCLE



BYTE READ CYCLE

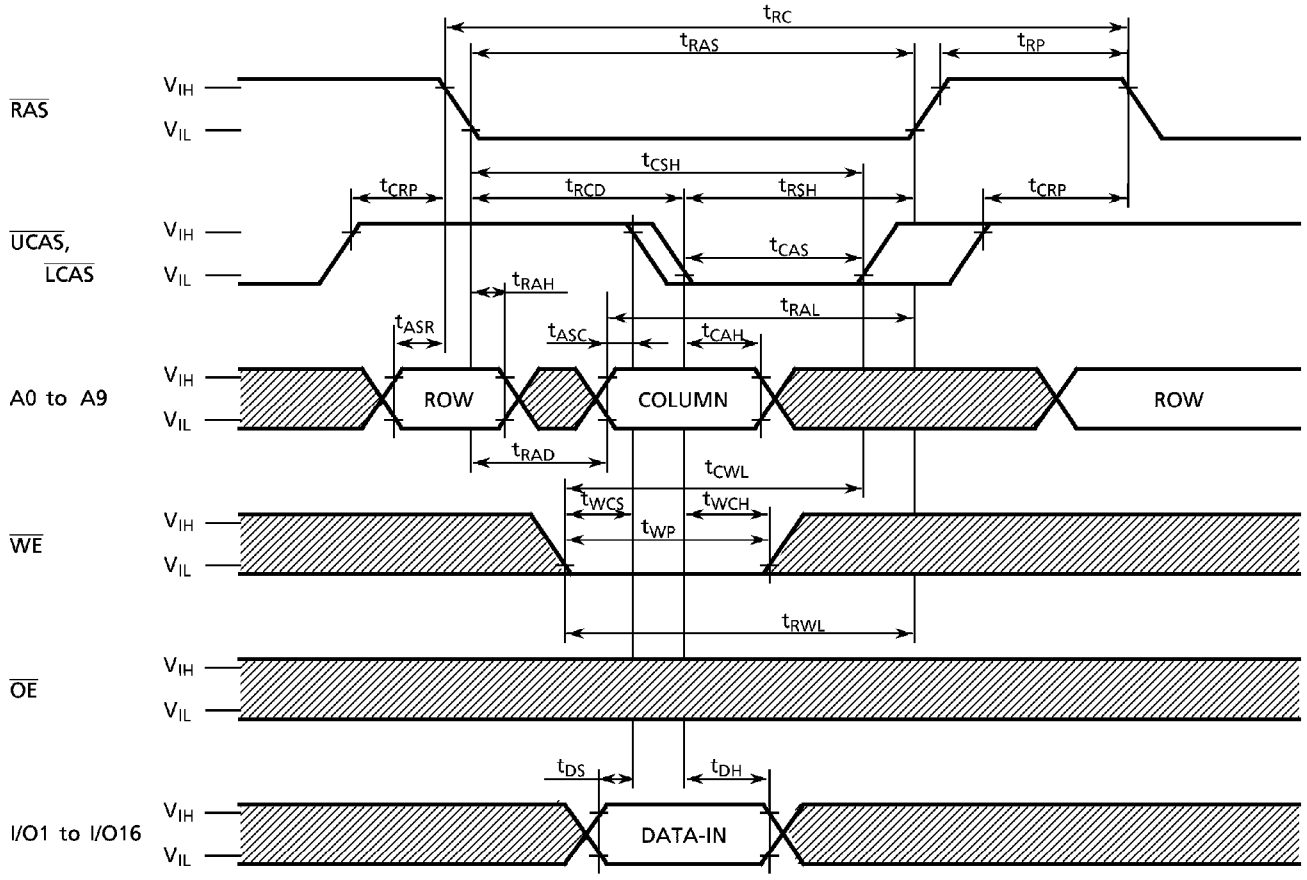


Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{IN} (I/O9 to I/O16) = Hi-Z
D_{OUT} (I/O1 to I/O8) = Hi-Z
(D_{IN} (I/O1 to I/O8) = Don't Care
D_{IN} (I/O9 to I/O16) = Hi-Z
D_{OUT} (I/O9 to I/O16) = Hi-Z)

: H or L

: Invalid Data

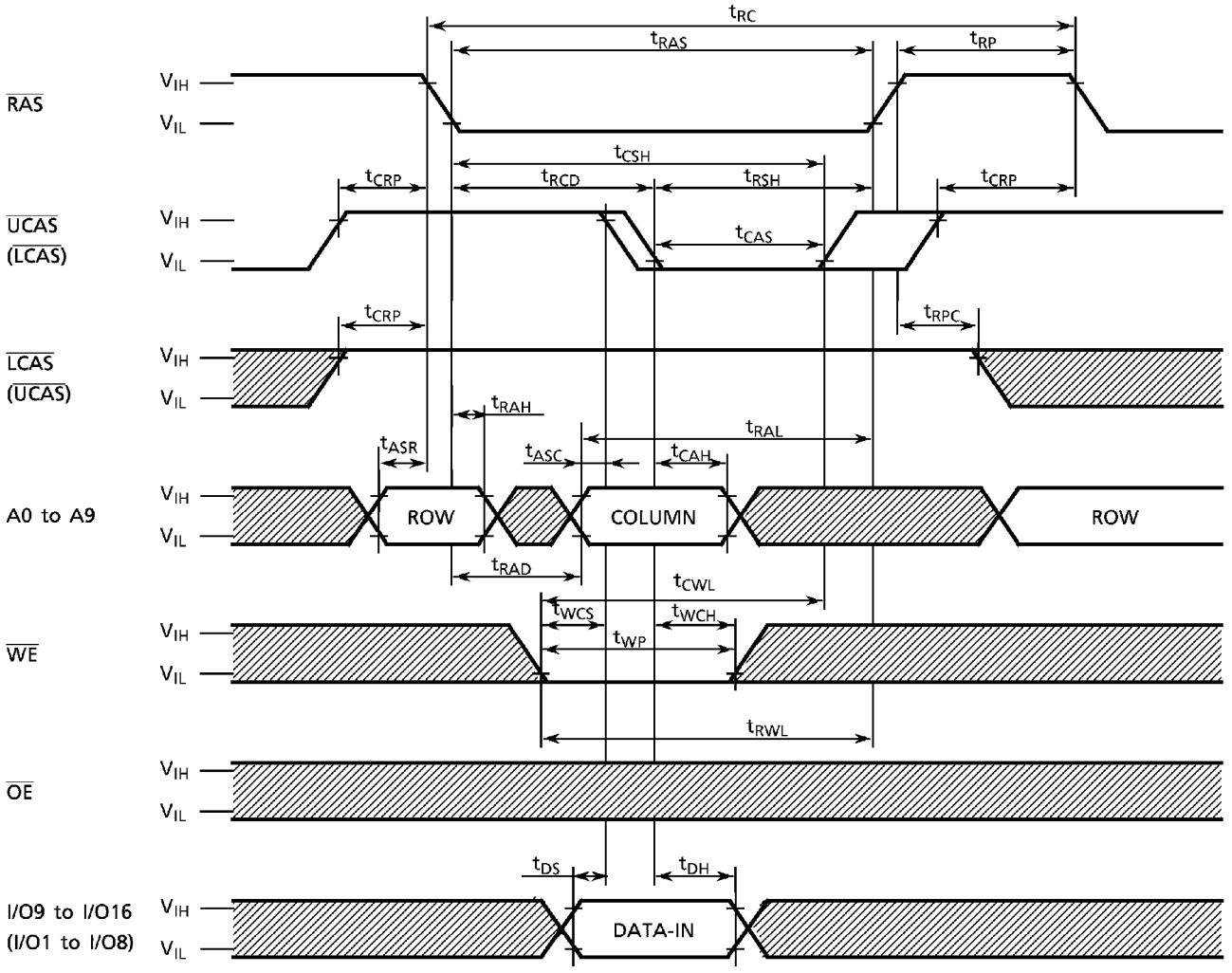
WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z

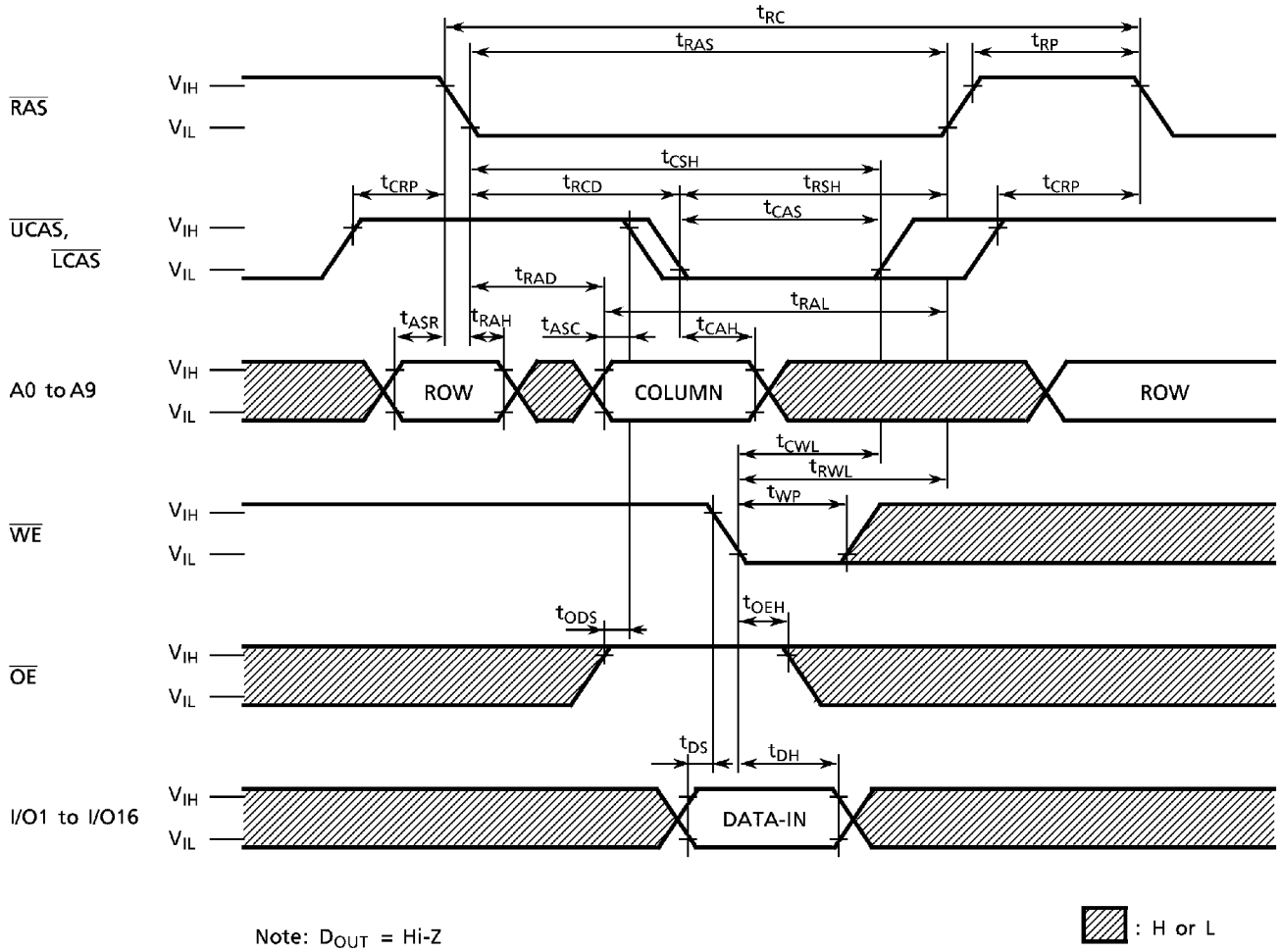
: H or L

BYTE WRITE CYCLE (EARLY WRITE)

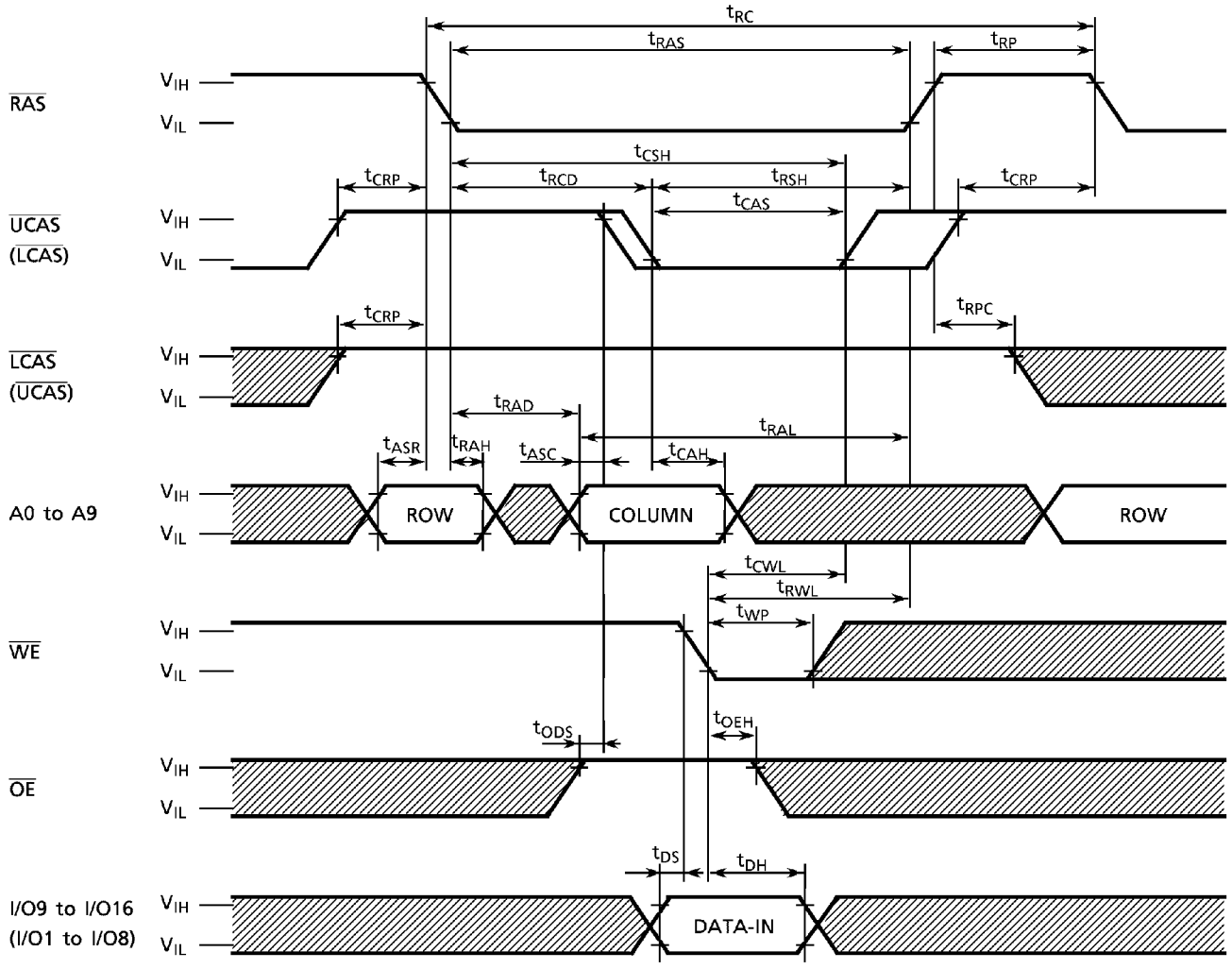


Note: D_{IN} (I/O1 to I/O8) = Don't Care
(D_{IN} (I/O9 to I/O16) = Don't Care)
D_{OUT} = Hi-Z

$\overline{OE}$-CONTROLLED WRITE CYCLE



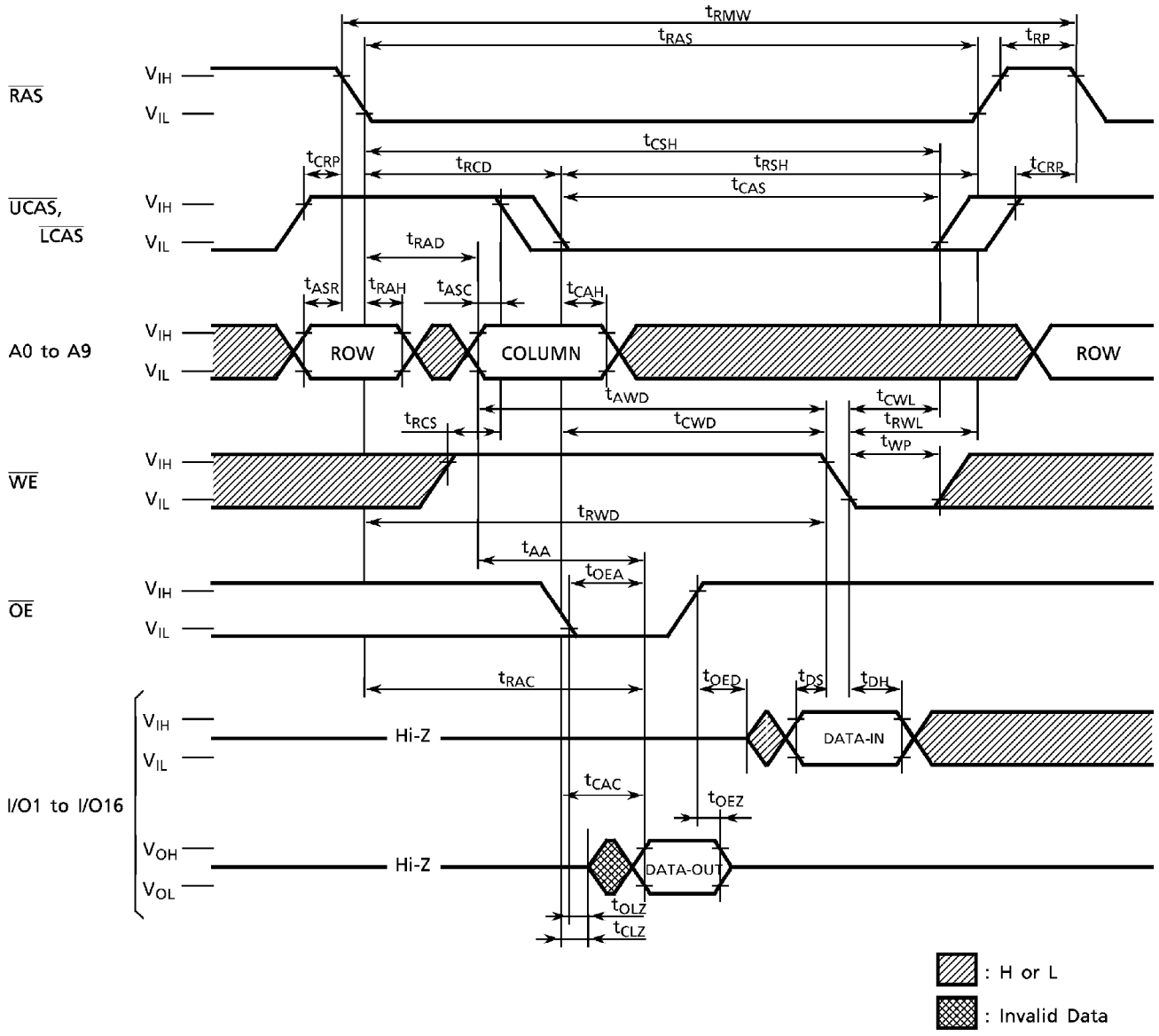
$\overline{OE}$-CONTROLLED BYTE WRITE CYCLE



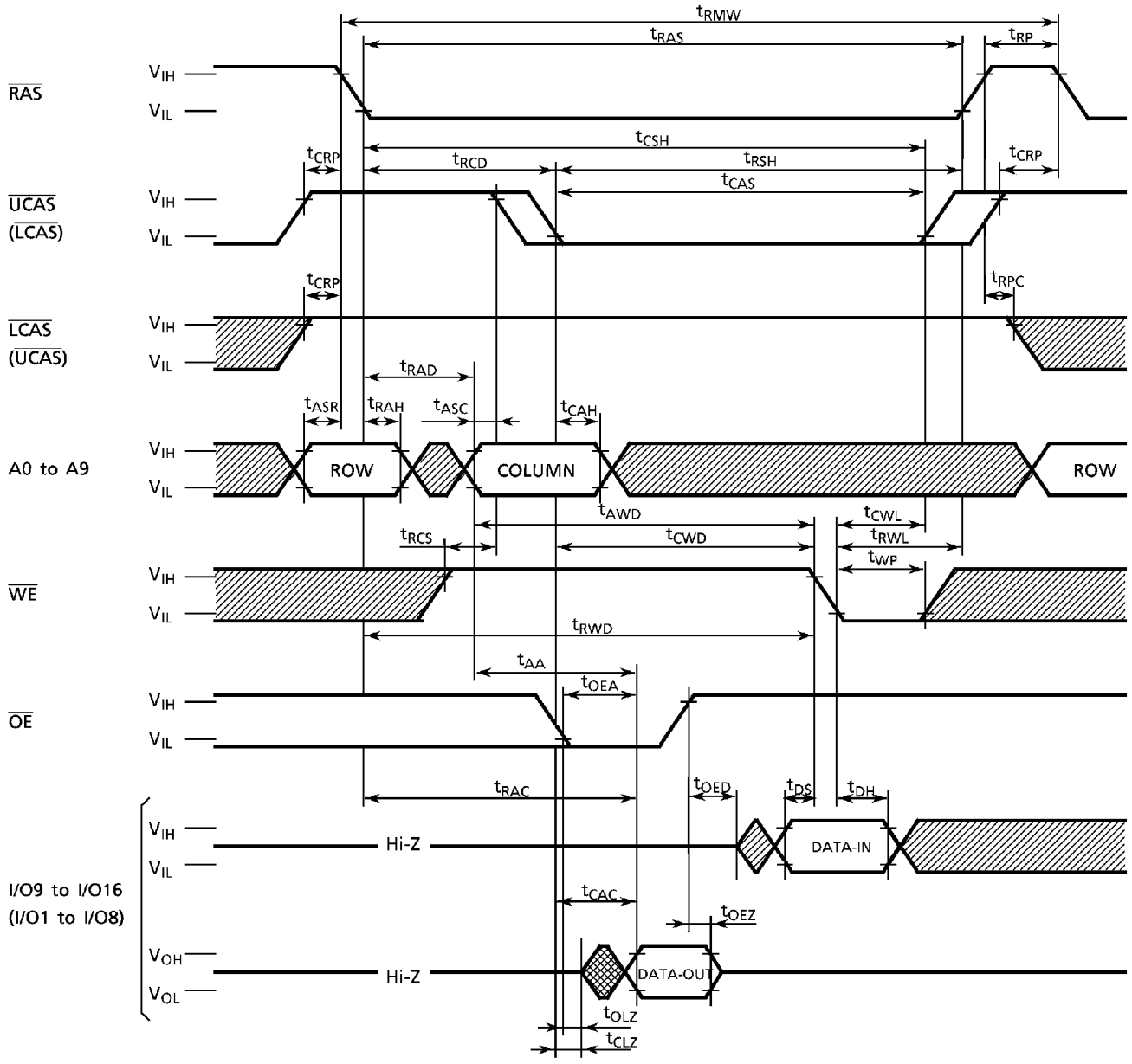
Note: D_{IN} (I/O1 to I/O8) = Don't Care
(D_{IN} (I/O9 to I/O16) = Don't Care)
D_{OUT} = Hi-Z

: H or L

READ-MODIFY-WRITE CYCLE



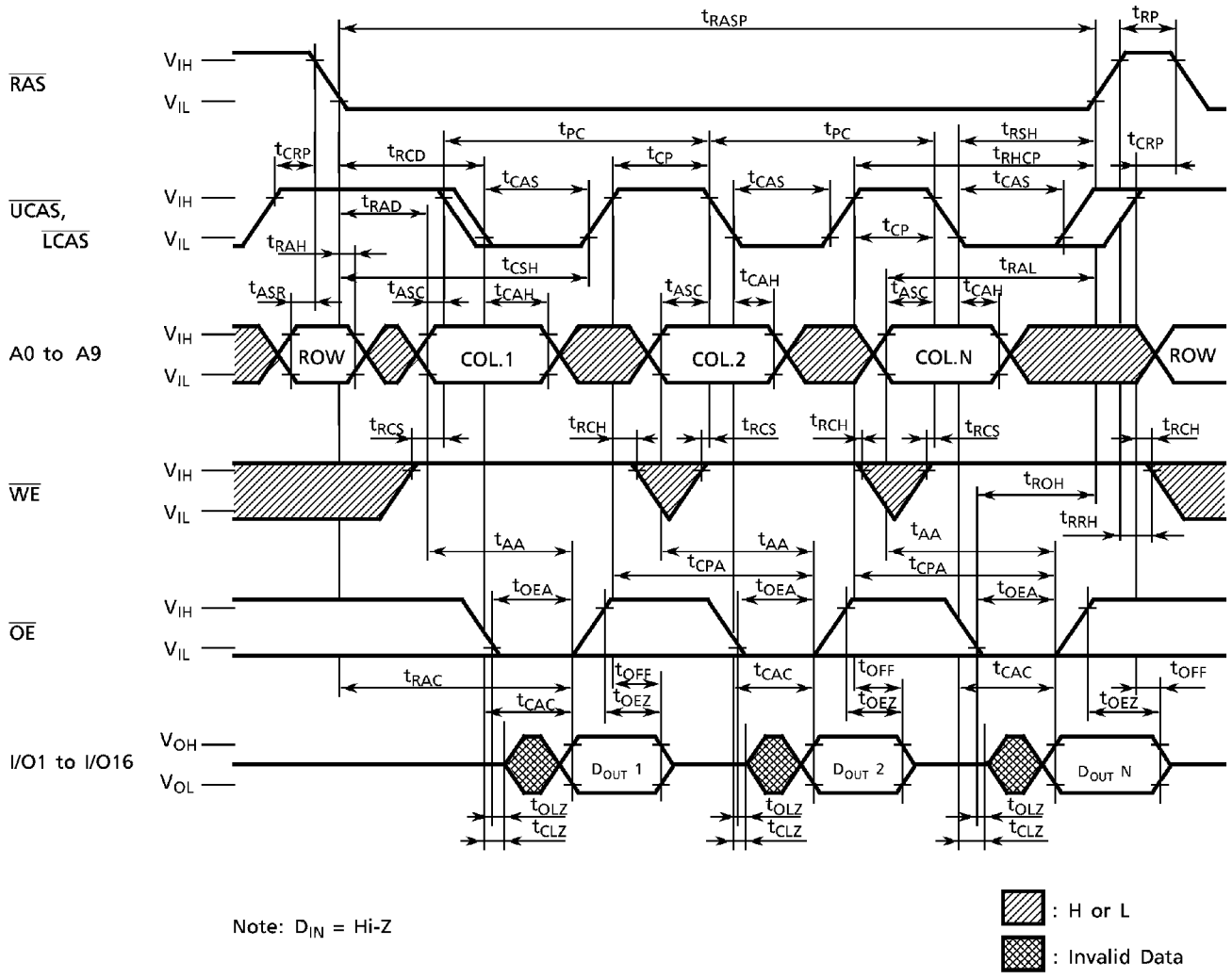
BYTE READ-MODIFY-WRITE CYCLE



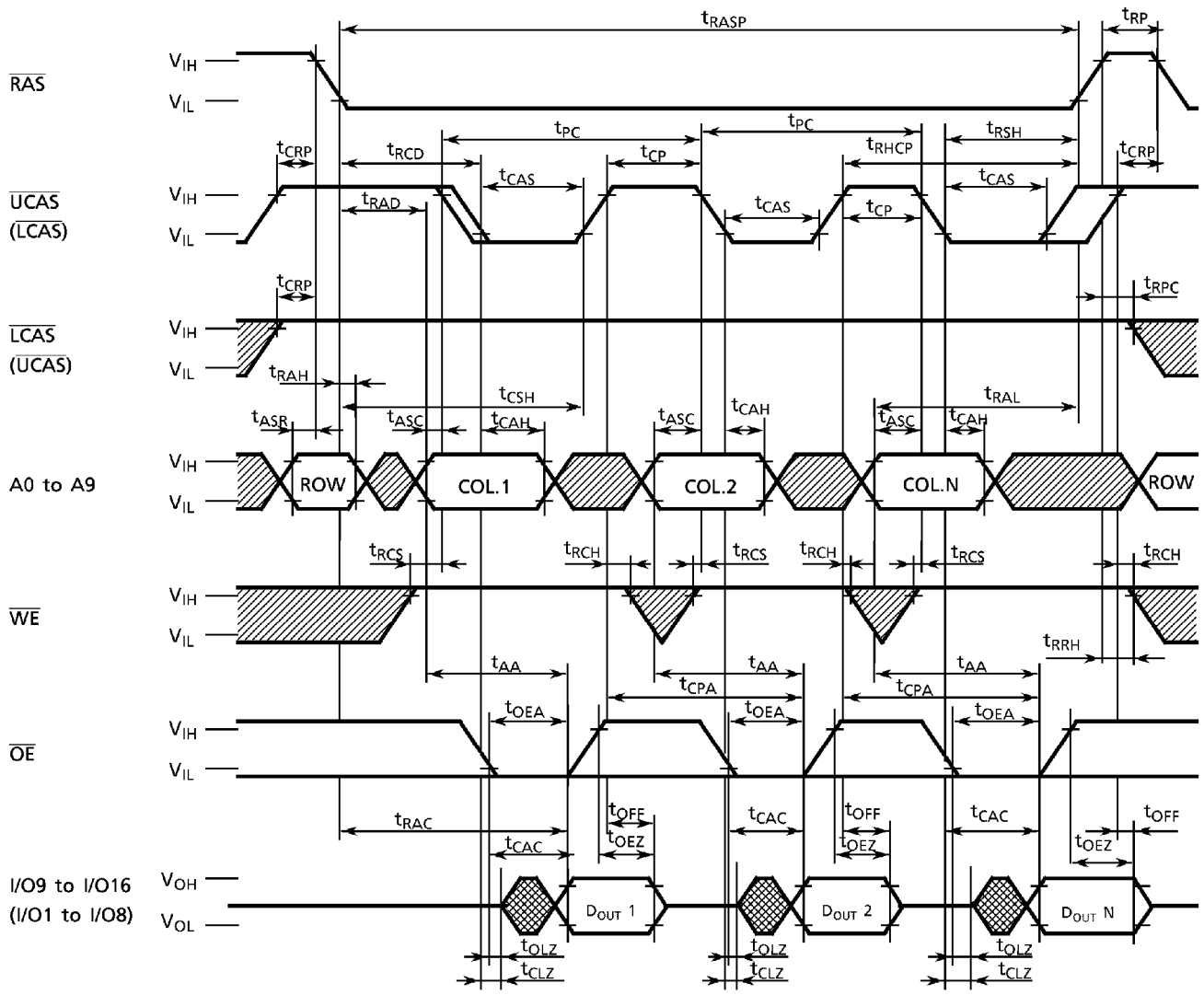
Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} (I/O1 to I/O8) = Hi-Z
(D_{IN} (I/O9 to I/O16) = Don't Care
D_{OUT} (I/O9 to I/O16) = Hi-Z)

: H or L
: Invalid Data

FAST PAGE MODE READ CYCLE



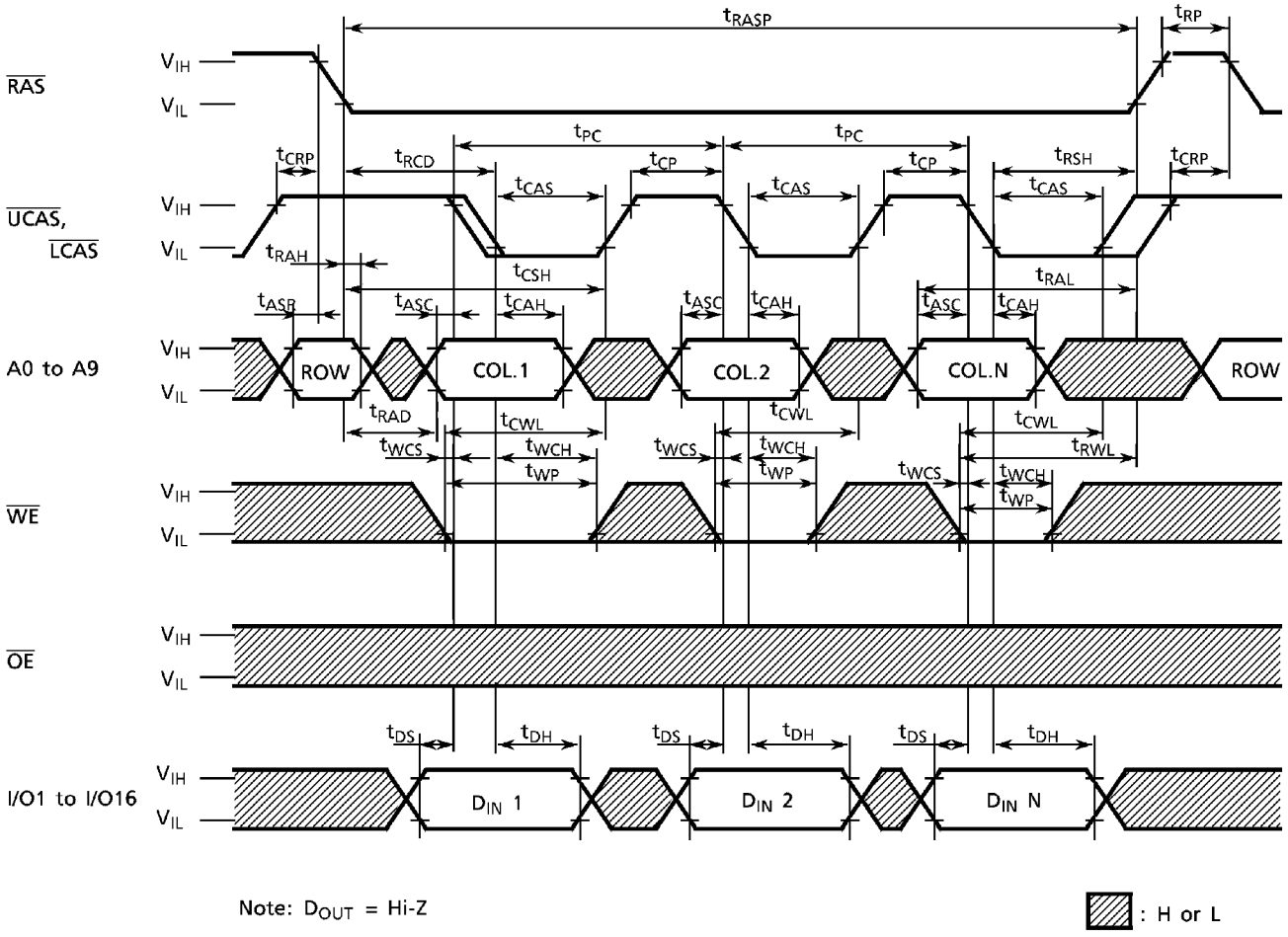
FAST PAGE MODE BYTE READ CYCLE



Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} (I/O1 to I/O8) = Hi-Z
(D_{IN} (I/O9 to I/O16) = Don't Care
D_{OUT} (I/O9 to I/O16) = Hi-Z)

: H or L
: Invalid Data

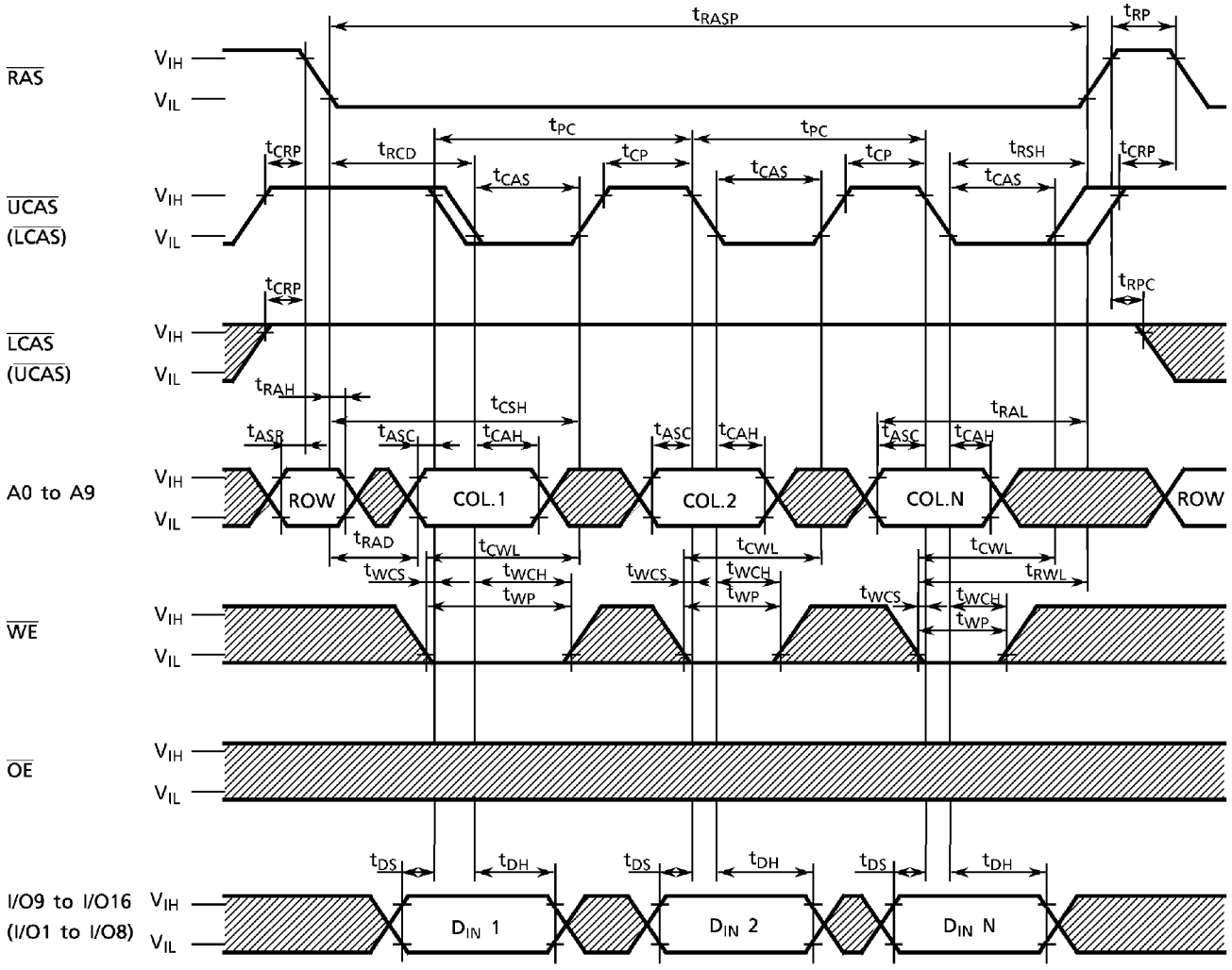
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



Note: D_{OUT} = Hi-Z

▨ : H or L

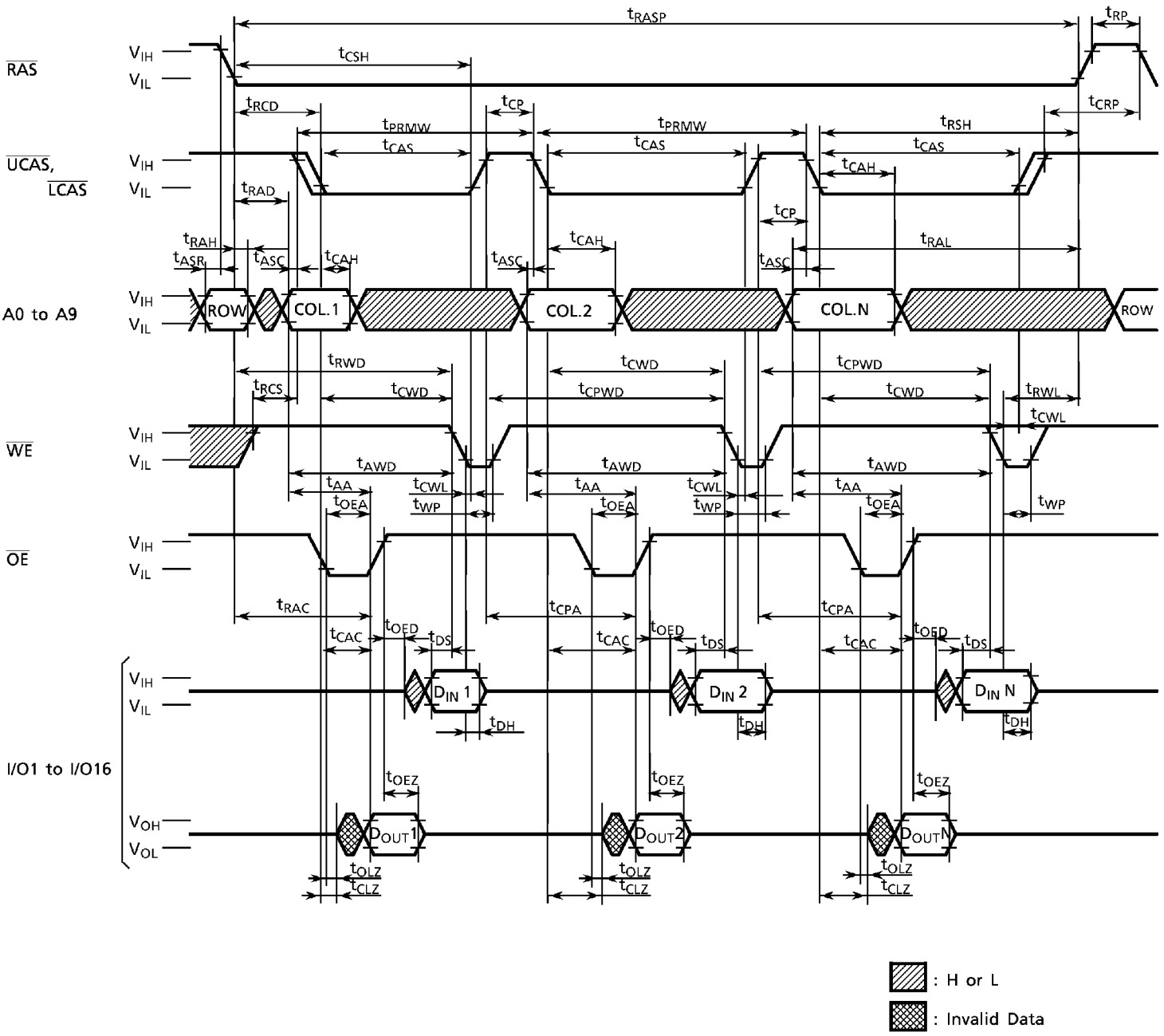
FAST PAGE MODE BYTE WRITE CYCLE (EARLY WRITE)



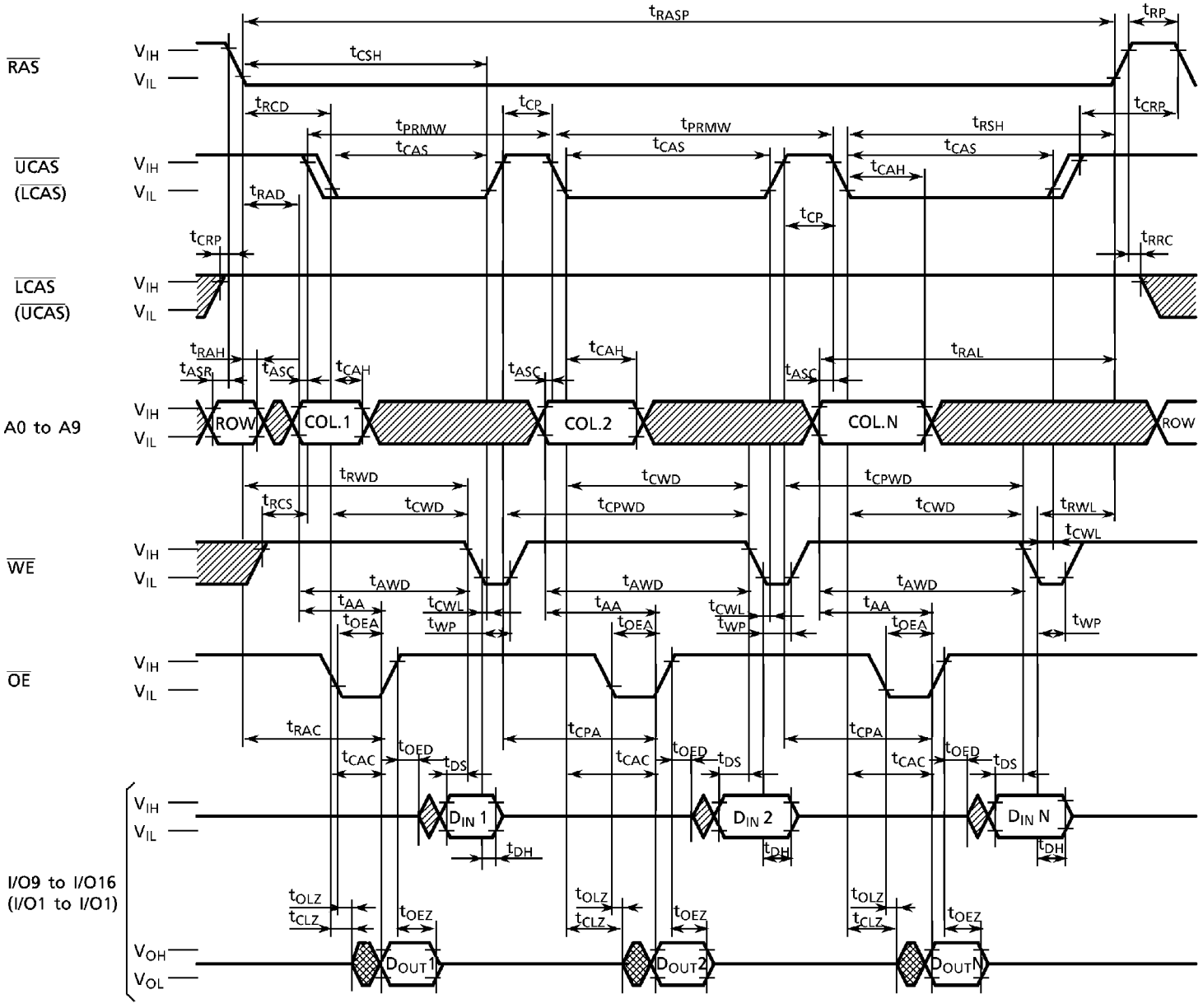
Note: D_{IN} (I/O1 to I/O8) = Don't Care
(D_{IN} (I/O9 to I/O16) = Don't Care)
D_{OUT} = Hi-Z

▨ : H or L

FAST PAGE MODE READ-MODIFY-WRITE CYCLE



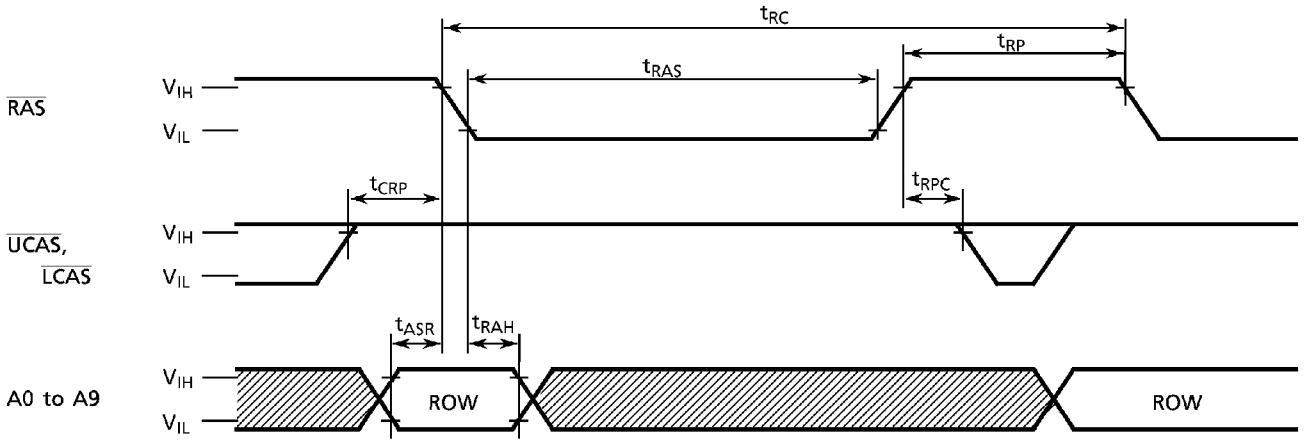
FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE



Note: D_{IN} (I/O1 to I/O8) = Don't Care
D_{OUT} (I/O1 to I/O8) = Hi-Z
(D_{IN} (I/O9 to I/O16) = Don't Care
D_{OUT} (I/O9 to I/O16) = Hi-Z)

: H or L
: Invalid Data

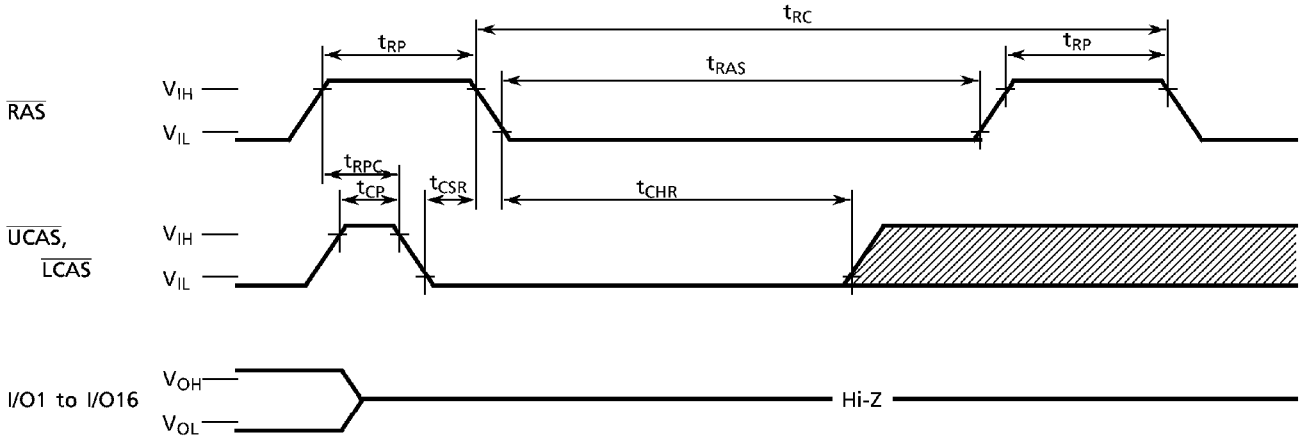
$\overline{RAS}$-ONLY REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$ = H or L
D_{IN} = H or L

: H or L

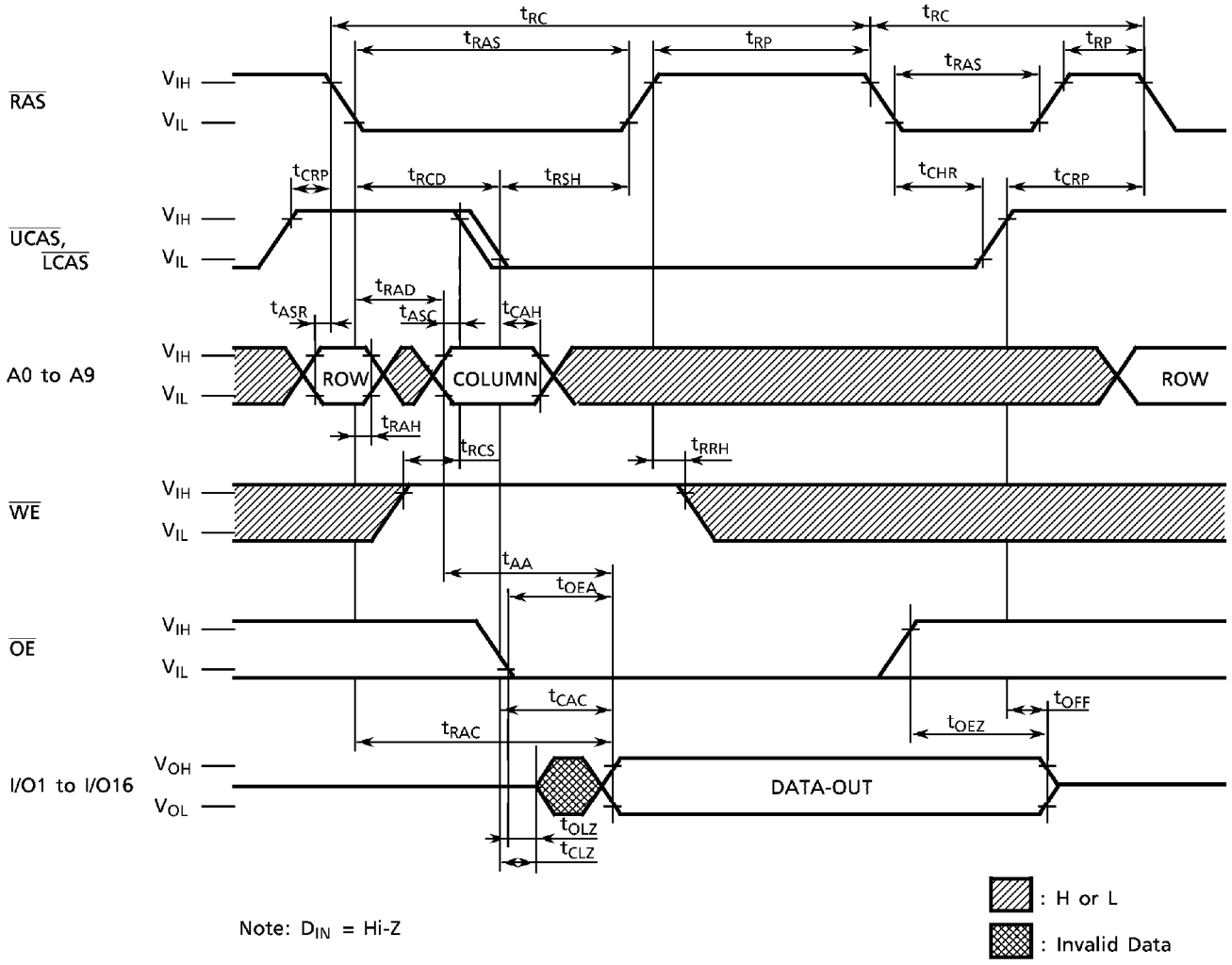
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A0 to A9 = H or L
D_{IN} = H or L

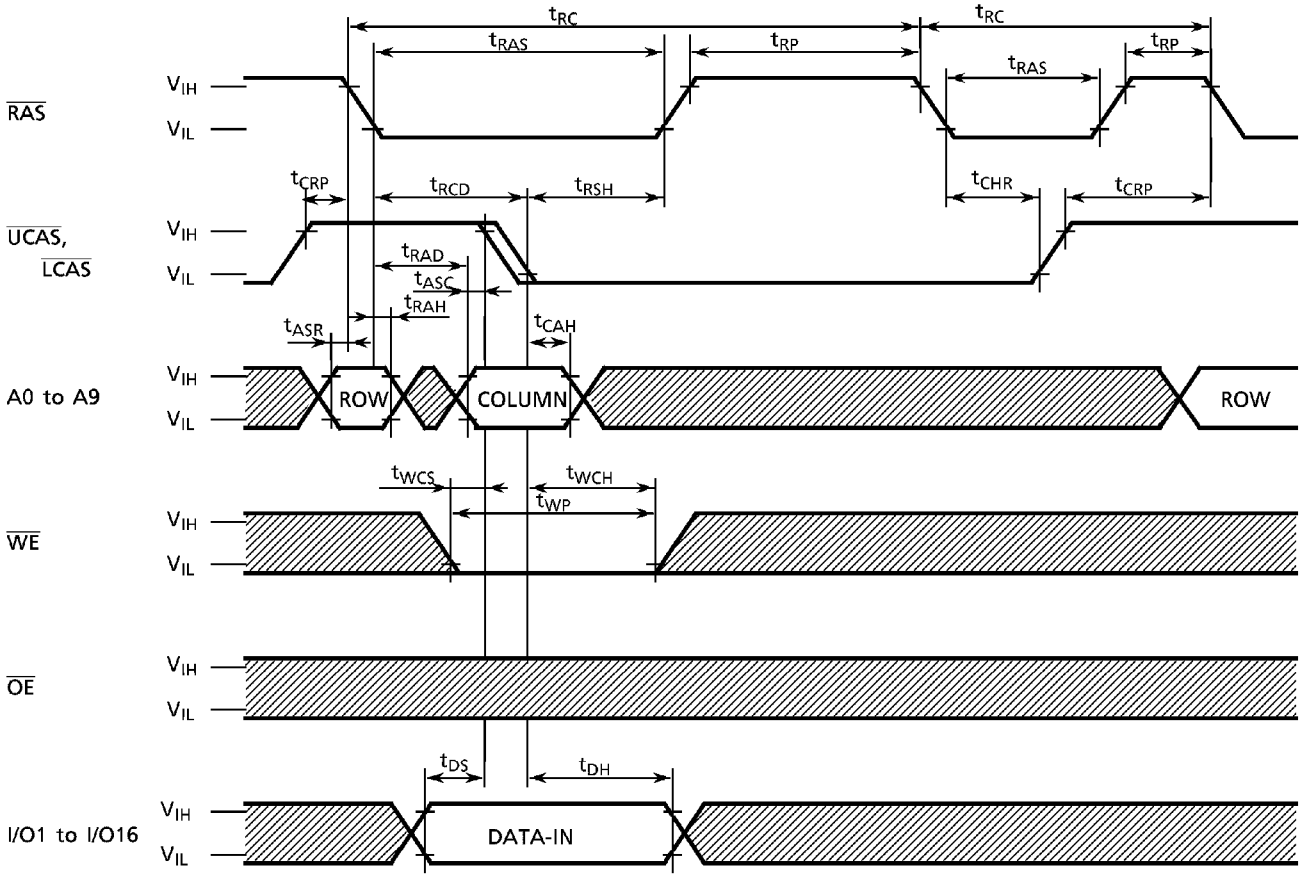
: H or L

HIDDEN REFRESH CYCLE (READ)



Note: D_{IN} = Hi-Z

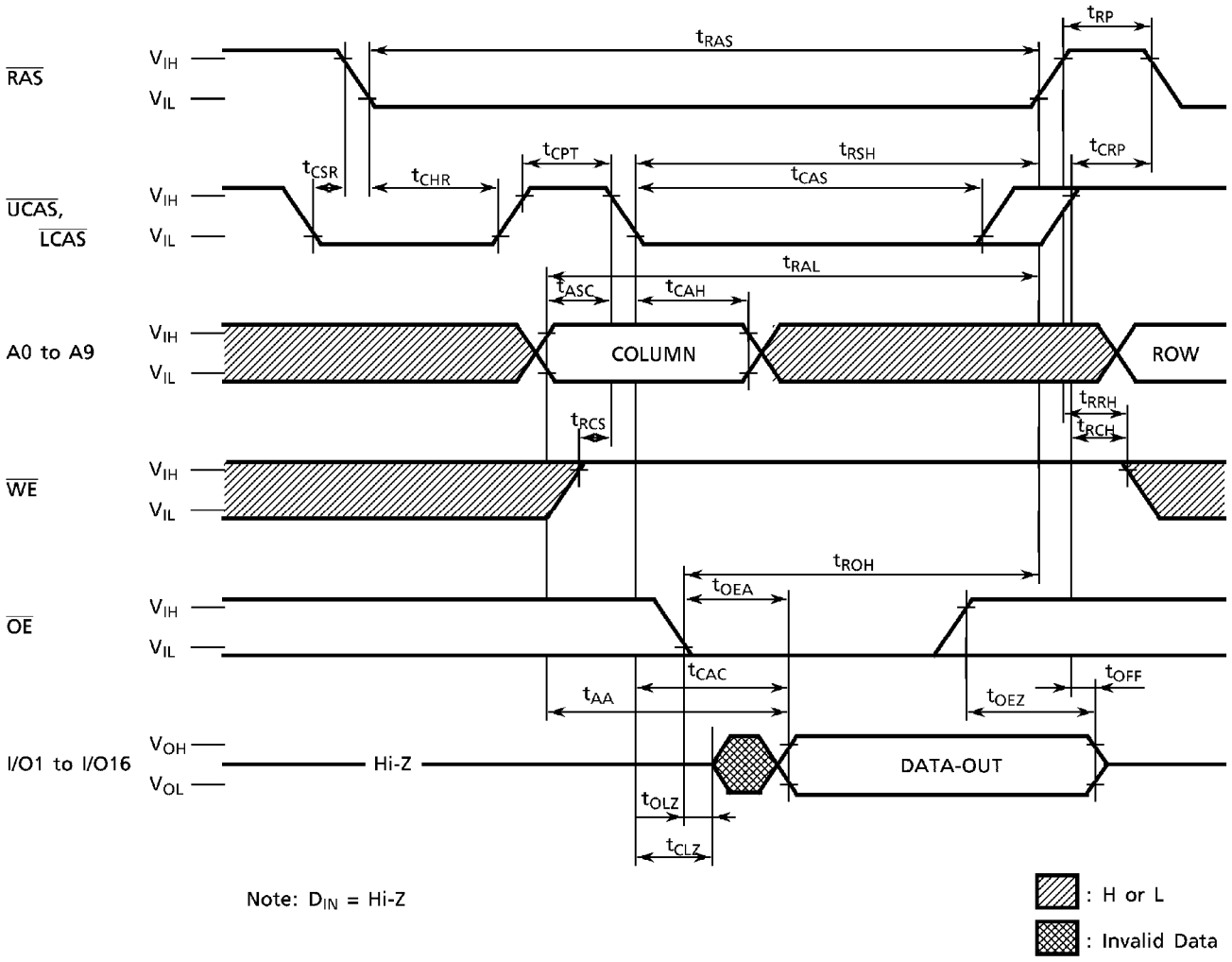
HIDDEN REFRESH CYCLE (WRITE)



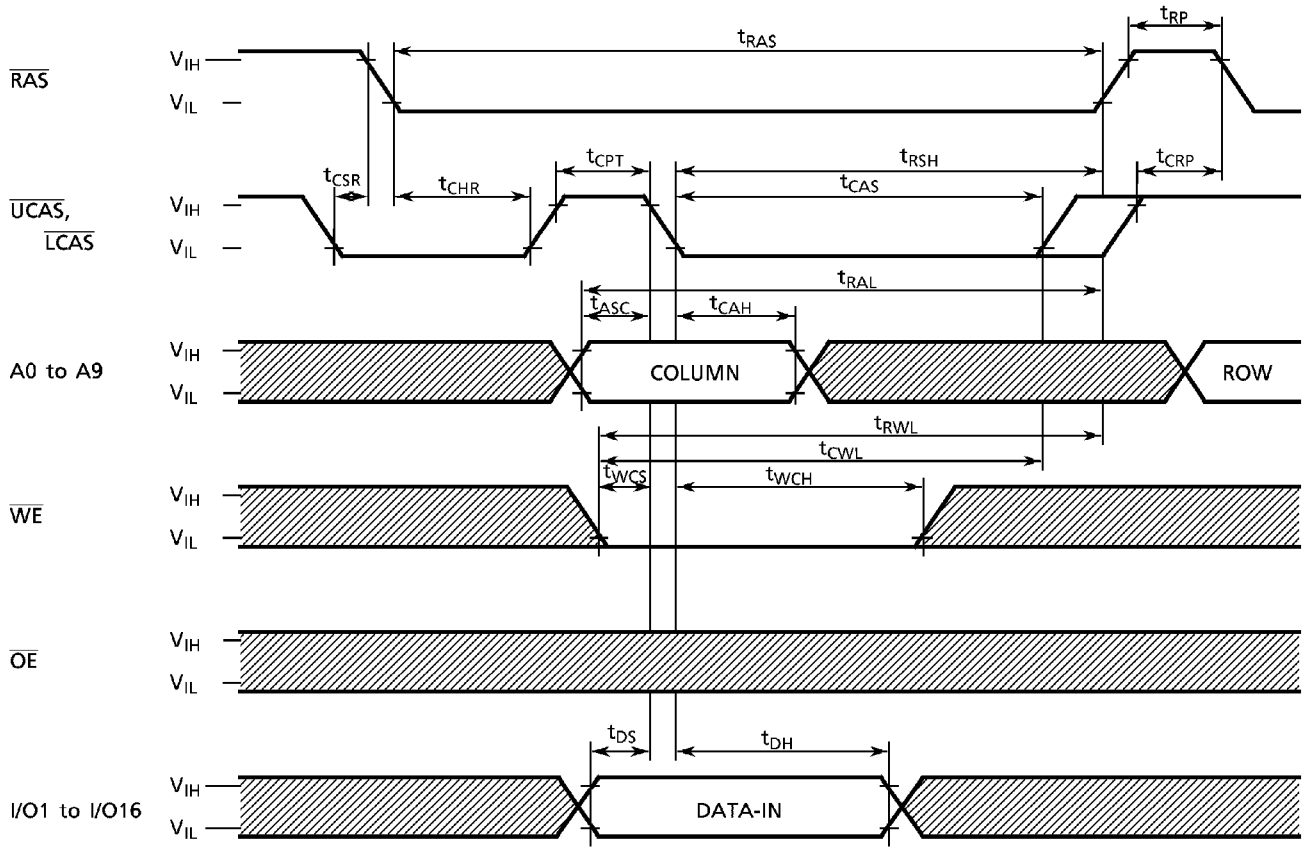
Note: D_{OUT} = Hi-Z

▨ : H or L

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH-COUNTER TEST READ CYCLE



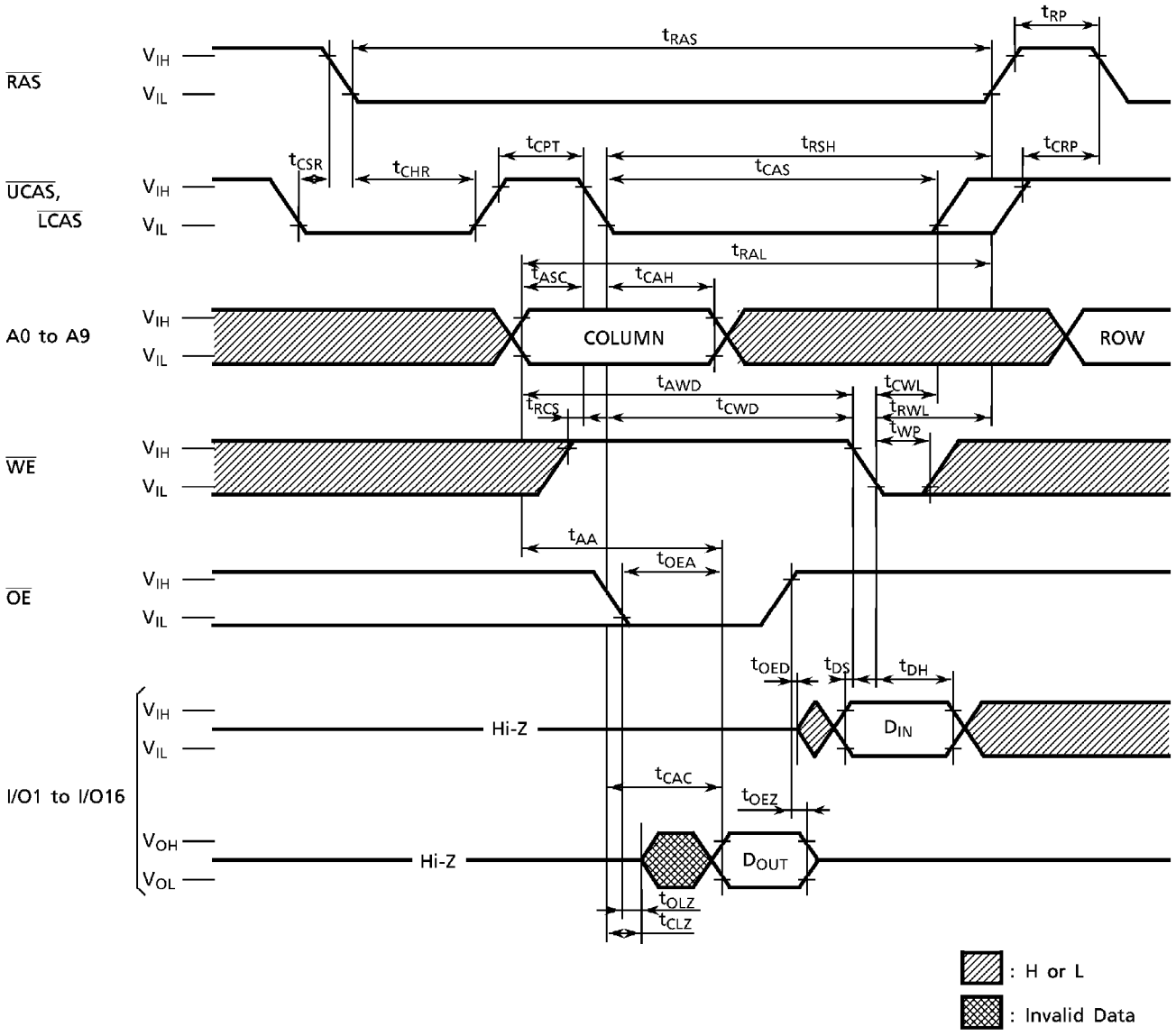
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH-COUNTER TEST WRITE CYCLE



Note: D_{OUT} = Hi-Z

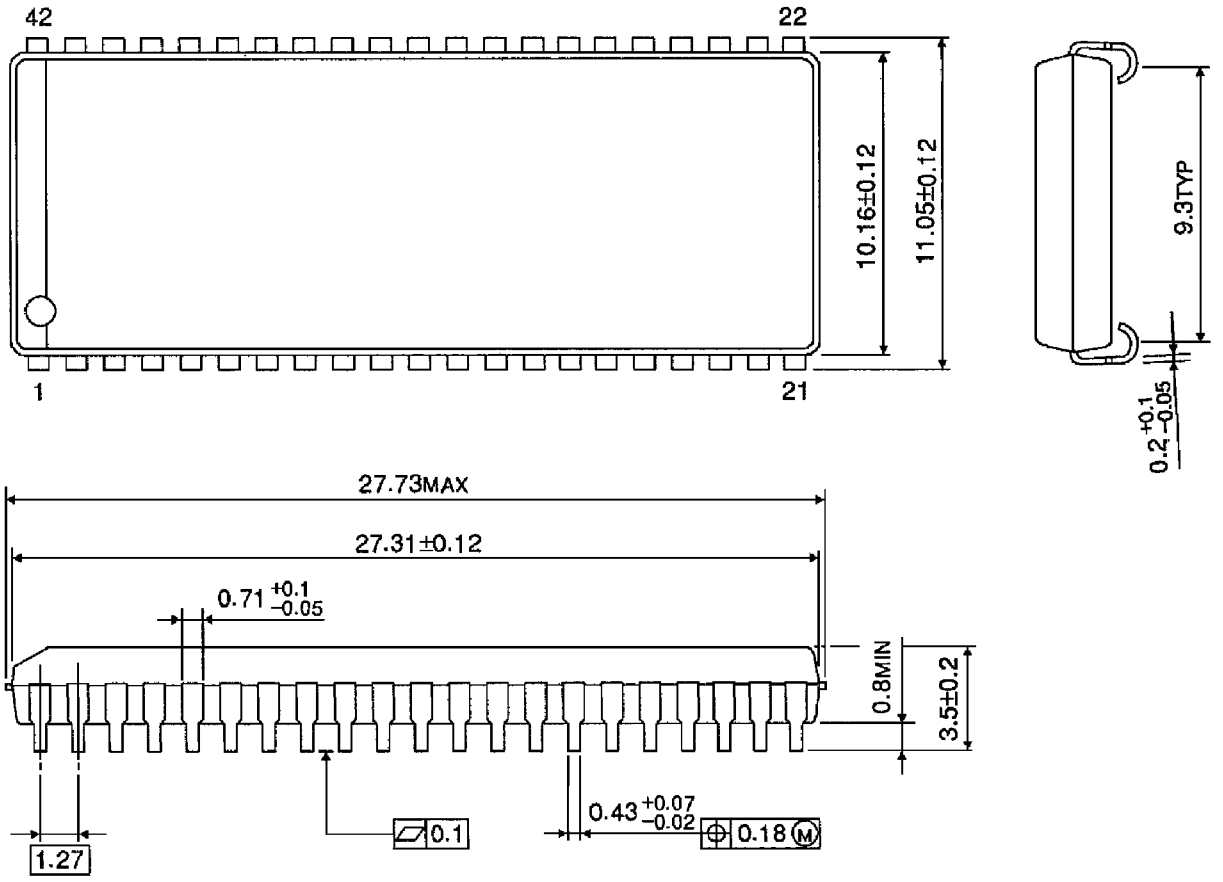
▨ : H or L

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH-COUNTER TEST READ-MODIFY-WRITE CYCLE



OUTLINE DRAWING (SOJ42-P-400-1.27)

Unit: mm



OUTLINE DRAWING (TSOPII 50/44-P-400-0.80)

Unit: mm