TOSHIBA

System ASIC
TC190 Series CMOS ASICs

0.6µ 3.0/3.3V ASIC Family

The 0.6µm, 5V TC190 ASIC series provides higher system performance and device integration with lower power than previous generation 5V families. Highly accurate delay models, area efficient memory cells and a very fine pitch TAB bonding capability for high I/O requirements are some of the features of the family which consists of Gate Array (TC190G), Embedded Array (TC190E) and Standard Cell (TC190C) ASIC products. The TC190E is a gate array based product that incorporates the ability to embed large diffused cell based hardmacrocells and compilable cells (RAM, ROM, DAC, multipliers, PLLs, etc) rather than building metalized functions. This enables denser, faster, higher performance ASICS to be designed while still exhibiting quick "gate array" type turn around times.

Benefits

- Advanced 0.6µ micron CMOS process with fast 240 gate delays.
- Reduction of gate power by as much as 20 percent over 0.8µm ASICs.
- 707,000 usable gates provide high levels of integration for improved performance and board area savings.
- Extensive libraries with a wide range of macrocells, compilable cells and megacells availible.
- Library compatible with existing TC160G/170G gate arrays for ease of design migration to 0.6µm technology
- Design Kit support for a wide range of EDA environments.
- VERILOG-XL sign off capability.
- 62µ TAB pad pitch allows higher number of I/O per gate than previous product generations.
- A wide range of packages are availible, including heat spreader plastic QFP, TABFP, BGA, tape BGA and others.
- New accurate delay modeling
- Verilog sign-off

System Performance

The high density, high performance TC190 series ASIC family is manufactured using Toshiba's 0.6µm double and triple layer complimentary metal-oxide silicon process. This family provides sub-micron ASIC density for pure 5V applications, and applications that are developed to transition over time to 3V. Typical applications are PC chipsets, graphics, telecommunications, networks, set top boxes and systems designed to migrate from 5V to 3V.

The 707K usable gates allow previously unobtainable levels of integration to be achieved on a 5V ASIC. The TC190 series supports many complex functions such as multipliers, DACs, ADCs,RAM, ROM and FIFOs.

The TC190 series offers Toshiba's high quality and high capacity manufacturing expertise. A partnership with Toshiba brings you not only the high quality and reliability ASICs, but fast prototype turnaround (3 day for gate array), steep production ramp-up and proven high volume manufacturing capacity.

Packaging

The TC190 series wide range of packaging options provide a packaging solution for any requirement. New packages are continuously being developed. Contact your Toshiba sales representative for the Toshiba Packaging Book for specific package/pin count information.

Features

TC190G	TC190E/C
– 22K – 707K usable gates	up to 730K
– 14 standard master sizes	21 standard master sizes
– up to 512 wire bonds	Same
– up to 776 TAB bond pads	
– 62µ Inner lead bond pads	Same
– Typical core power – 2.63µW/gate/Mhz	
– 180+ primitive cells (scan, standard, high drive cells)	Same
– 450+ I/O cells including (hign drive {24mA} slew rate control high speed output buffers)	Same
Compiled cells – sync/async single, dual, triple port RAM, ROM	Same
– Hard macrocells including those for PCI bus interface are availible. Some fast multipliers, adders, ALUs, UARTS timers and special I/O cells are in development.	
– Ability to embed large Compilable, fully diffused memory blocks provide higher performance and increased desnsity.	Same

TC190G Two Input NAND Gate Delay Performance

ND2 Gate Delay[1]	Fanout = 2	Fanout = 4	Fanout = 6
Typical[2]	240ps	336ps	432ps
Worst Case[3]	406ps	568ps	731ps

Power Dissipation

at 5V	**Power = 2.63µW/gate/MHz**

NOTE 1: These typical numbers are for estimation purposes only. Power dissapation is dependent on wire loading and gate switching rates.

TC190G Gate Array Product Summary

Reference	Usable Gates		I/O Pads		
	DLM	TLM	Wirebond Pads	TAB 62μm	TAB 83μm
TC190G02/ 52	12,000	22,000	80	160	120
TC190G04/ 54	22,000	38,000	104	208	156
TC190G06/ 56	31,000	54,000	128	256	192
TC190G08/ 58	39,000	68,000	144	296	220
TC190G10/ 60	47,000	81,000	160	324	240
TC190G12/ 62	56,000	99,000	176	356	264
TC190G14/ 64	67,000	117,000	192	388	288
TC190G16/ 66	82,000	143,000	208	428	320
TC190G20/ 70	98,000	171,000	240	—	368
TC190G24/ 74	125,000	219,000	272	—	416
TC190G32/ 82	175,000	307,000	336	—	512
TC190G36/ 86	228,000	400,000	384	—	584
TC190G40/ 90	288,000	505,000	432	—	656
TC190G42/ 92	404,000	707,000	512	—	776

* Double Layer Metal / Triple Layer Metal

TC190E/C Embedded Array and Standard Cell Product

Reference	Usable Gates		I/O Pads		
	DLM	TLM	Wirebond Pads	TAB 62μm	TAB 83μm
TC190E/C02	12,000	—	80	152	112
TC190E/C04	21,000	—	104	200	148
TC190E/C06	32,500	—	128	248	186
TC190E/C08/58	40,900	66,450	144	288	212
TC190E/C10/60	49,300	80,200	160	316	236
TC190E/C12/62	59,950	97,450	176	348	260
TC190E/C14/64	71,600	116,350	192	380	284
TC190E/C16/66	81,050	131,450	208	420	312
TC190E/C18/68	94,000	152,400	224	—	336
TC190E/C20/70	107,850	174,900	240	—	360
TC190E/C22/72	122,700	198,950	256	—	384
TC190E/C24/74	138,500	224,600	272	—	408
TC190E/C26/76	155,250	251,750	288	—	432
TC190E/C28/78	172,950	280,450	304	—	456
TC190E/C30/80	181,250	295,200	320	—	480
TC190E/C32/82	199,800	325,400	336	—	504
TC190E/C34/84	229,350	373,500	360	—	540
TC190E/C36/86	260,900	424,950	384	—	576
TC190E/C38/88	294,500	479,650	408	—	612
TC190E/C40/90	330,150	537,700	432	—	648
TC190E/C42/92	437,150	728,550	512	—	768

* Double Layer Metal / Triple Layer Metal

Clock Distribution Network

Toshiba implements clock distribution networks in ASIC designs using a variety of different topologies including loop, grid, tree or trunk. The actual topology used depends on the desired clock skew specification and other design criteria such as power consumption limits and availible gates. Typical on-chip skew delays will be less than 0.5ns. Toshiba plans to offer tighter links between logical and physical; design processes, i.e. synthesis, floor planning and layout, which will further enable designers to optomize their designs.

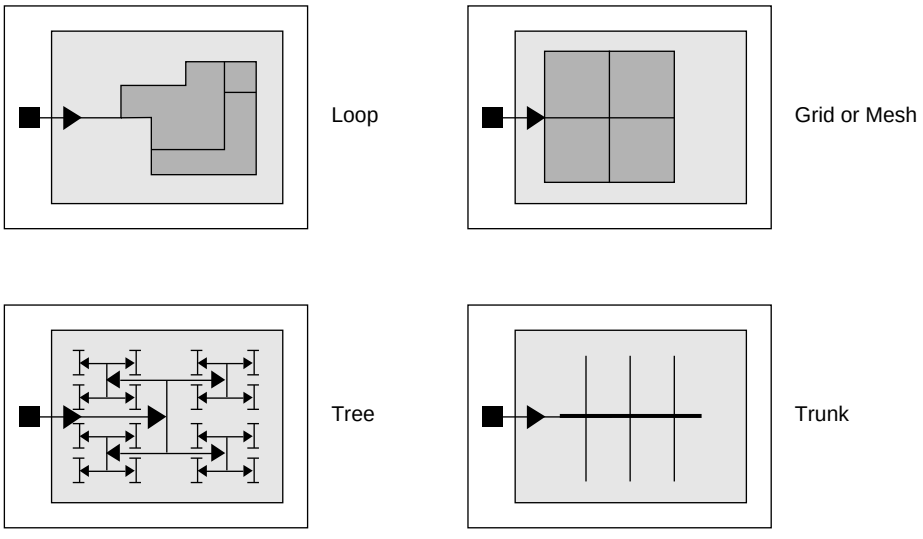
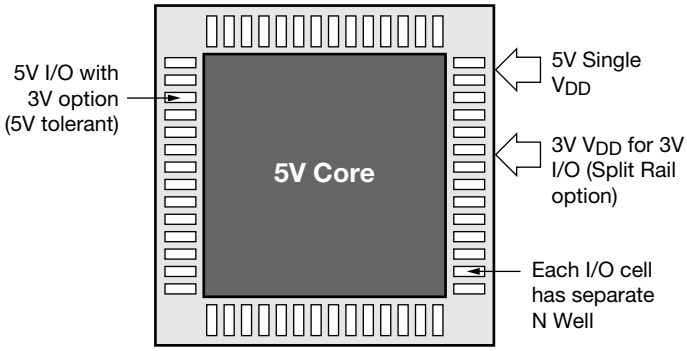


Figure 1. Clock Delay and Skew Control Layout Topologies

TC190 Series Architecture

Advantages

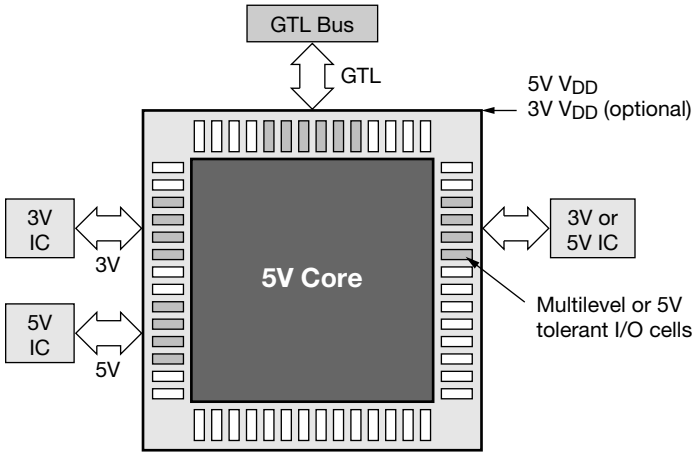
- 3V I/O available with 3Volt V_{DD} option
- 3V/5V I/O buffer V_{DD} can be switched if required
- No restrictions on 3/5V I/O placement



TC190 Series Mixed Voltage Interface Option

Applications

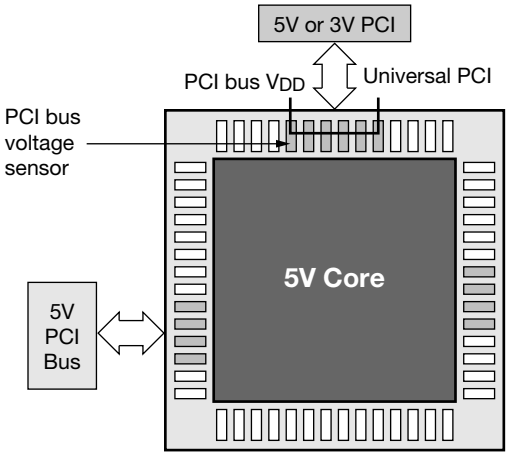
- PC chipsets
- Graphics
- Telecommunications
- Networks
- Set Top boxes
- Systems designed to migrate from 5V to 3V memory



TC190 Series PCI Interface Option

Universal PCI Buffers

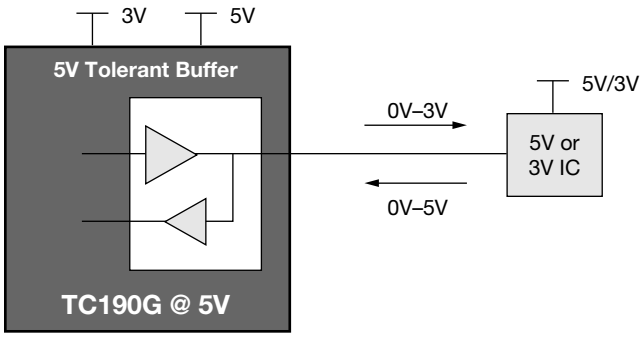
- Will interface to 5V or 3V PCI bus
- Change levels dependent on bus V_{DD}
- No restrictions on I/O placement



5V Tolerant I/Os

5V Tolerant Interface

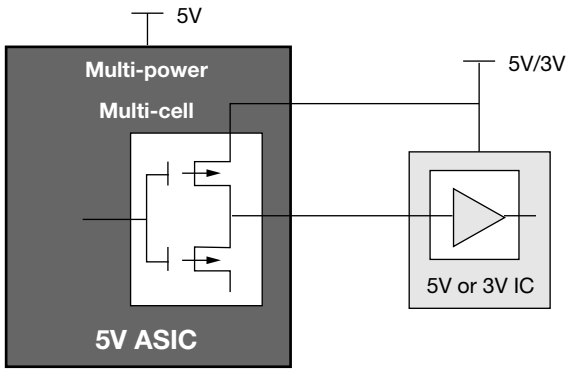
- 5V tolerant:
  OUTPUT: 0V–3V output level could be connected to 5V bus
  INPUT: 0V–5V input level could be connected to 5V bus
- No placement restrictions



Mixed 3V/5V Support

Multilevel Interface Cell Technology – TC160G/TC170G (TC190G)

- 5V/3V full level interface with multi-power
- High speed operation:
  Driver: T_{pd}: 6ns max (high speed type) @ 50pF load
  Receiver: T_{pd}: 4ns max @ F0=5
- No placement restrictions
- Power sequence requirement: 5V, then 3V



EDA Libraries and Design Kits

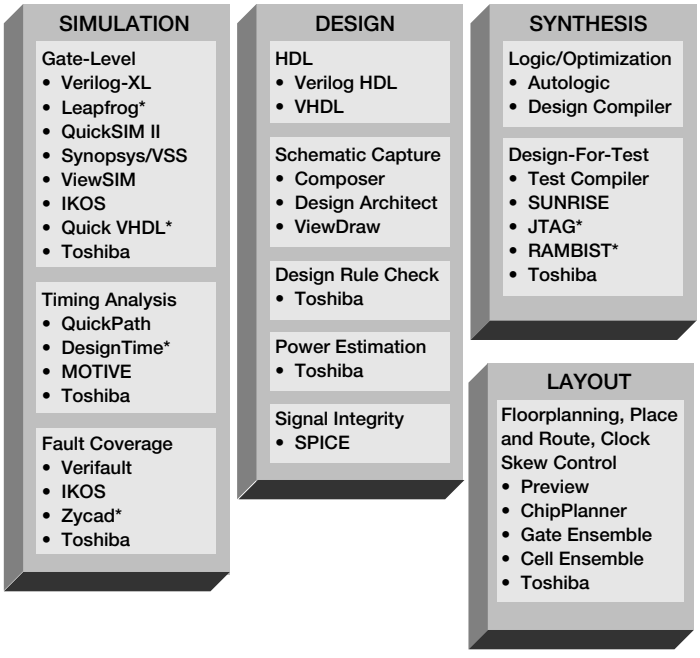
The TC190 series is supported by two design environments:

– The Toshiba traditional EDA system based on distriputed delay models

– The Toshiba Non-Linear Delay Model (NDM), which uses pin to pin timing and table lookup while taking into account the input slew rate as well as output load capacities.

Designers can use the traditional EDA option or the Verilog NDM sign-off system for the TC190 series. The libraies are upward compatible with the Toshiba 0.8µm ASIC family, thus reducing the effort needed when transferring a design from 0.8µm to 0.6µ technologies.

Toshiba Design Environment II



* In development

AS31700496

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