

SILICON GATE CMOS

32,768 WORD x 16 BIT CMOS PSEUDO STATIC RAM

Description

The TC511632FL/FTL is a 512K bit high speed CMOS pseudo static RAM organized as 32,768 words by 16 bits. The TC511632FL/FTL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC511632FL/FTL operates from a single 5V power supply. Refreshing is supported by a refresh (RFSH) input which enables two types of refreshing - auto refresh and self refresh. The TC511632FL/FTL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of WE thus simplifying the microprocessor interface.

The TC511632FL/FTL is available in a 40-pin small outline plastic flat package and a 44-pin outline (40 actual pins) plastic thin small outline package (forward type).

Features

- Organization: 32,768 words x 16 bits
- Single 5V power supply
- Fast access time

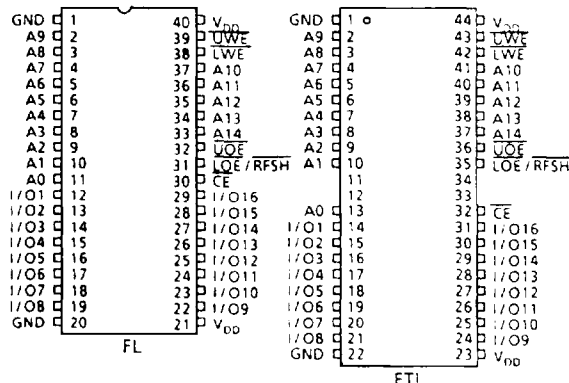
	TC511632FL/FTL		
	-70	-85	-10
t_{CEA} $\overline{CE}$ Access Time	70ns	85ns	100ns
t_{OEA} $\overline{OE}$ Access Time	30ns	35ns	40ns
t_{RC} Cycle Time	115ns	135ns	160ns
Power Dissipation	440mW	385mW	330mW
Self Refresh Current	100 μ A		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 256 refresh cycles/4ms
- Package
 - TC511632FL: SOP40-P-525
 - TC511632FTL: TSOP44-P-400B

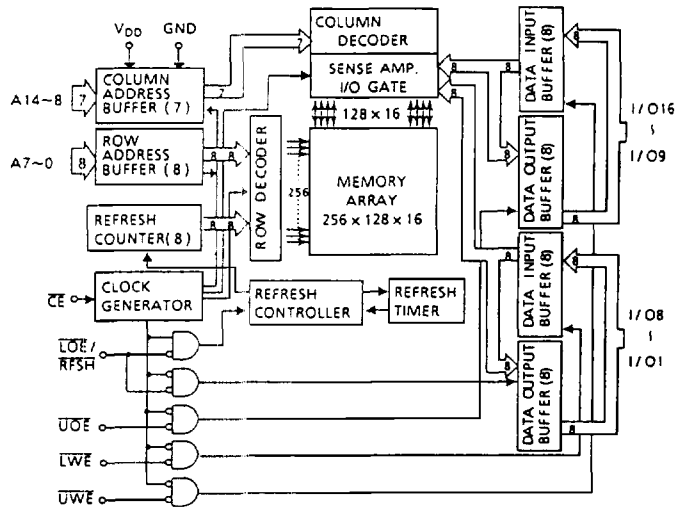
Pin Names

A0 ~ A14	Address Inputs
$\overline{UWE}$	Upper Byte Write Enable Input
$\overline{LWE}$	Lower Byte Write Enable Input
$\overline{UOE}$	Upper Byte Output Enable Input
$\overline{LOE/RFSH}$	Lower Byte Output Enable Input Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ~ I/O16	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	CE	UOE	LOE/RFSH	UWE	LWE	A0 ~ A14	I/O9 ~ 16	I/O1 ~ 8
Standby		H	*	*	*	*	*	HZ	HZ
Read (Word)		L	L	L	H	H	V*	D _{OUT}	D _{OUT}
Read (Upper Byte)		L	L	H	H	H	V*	D _{OUT}	HZ
Read (Lower Byte)		L	H	L	H	H	V*	HZ	D _{OUT}
Read (HZ)		L	H	H	H	H	V*	HZ	HZ
Write (Word)		L	*	*	L	L	V*	D _{IN}	D _{IN}
Write (Upper Byte)		L	*	H	L	H	V*	D _{IN}	*
Write (Lower Byte)		L	H	*	H	L	V*	*	D _{IN}
Don't Use		L	*	L	L	H	*	-	-
Don't Use		L	L	*	H	L	*	-	-
CE only Refresh			H		H	H	V*	HZ	HZ
Auto/Self Refresh		H	*		*	*	*	HZ	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of CE, all address inputs are latched. At all other times, the address inputs are "**".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V _{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V _{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V _{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T _{OPR}	Operating Temperature	0 ~ 70	°C	
T _{STRG}	Storage Temperature	-55 ~ 150	°C	
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P _D	Power Dissipation	600	mW	
I _{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	

DC Characteristics ($T_a = 0 \sim 70^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) $\overline{CE}$, Address cycling: $t_{11C} = t_{10C}$ min.	70ns version	—	60	80	mA 3, 4
		85ns version	—	50	70	
		100ns version	—	40	60	
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, All other pins = V_{IH} or V_{IL}	—	—	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, All other pins = $V_{DD} - 0.2V$ or $0.2V$	—	—	100	μA	
I_{DDF1}	Self Refresh Current (Average) $\overline{CE} = V_{IH}$, $\overline{LOE}/\overline{RFSH} = V_{IL}$, All other pins = V_{IH} or V_{IL}	—	—	1	mA	
I_{DDF2}	Self Refresh Current (Average) $\overline{CE} = V_{DD} - 0.2V$, $\overline{LOE}/\overline{RFSH} = 0.2V$, All other pins = $V_{DD} - 0.2V$ or $0.2V$	—	50	100	μA	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other inputs not under test = $0V$	—	—	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled ($\overline{CE} = V_{IH}$ or $\overline{LOE}/\overline{RFSH} = V_{IH}$ or $\overline{LWE} = V_{IL}$) $0V \leq V_{OUT} \leq V_{DD}$ $\overline{UOE} = V_{IH}$ $\overline{UWE} = V_{IL}$	—	—	± 10	μA	
V_{OH}	Output High Level $I_{OH} = -1mA$	2.4	—	—	V	
V_{OL}	Output Low Level $I_{OL} = 2.1mA$	—	—	0.4	V	

Capacitance* ($V_{DD} = 5V$, $T_a = 25^\circ\text{C}$, $f = 1MHz$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A14)	—	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{LOE}/\overline{RFSH}$, $\overline{UOE}$, $\overline{LWE}$, $\overline{UWE}$)	—	7	
C_{IO}	Input/Output Capacitance	—	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%) (Notes: 5, 6, 7, 8, 13)

SYMBOL	PARAMETER	-70		-85		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	135	—	160	—	ns	
t _{RMW}	Read Modify Write Cycle Time	175	—	190	—	220	—		
t _{CE}	$\overline{\text{CE}}$ Pulse Width	70	10,000	85	10,000	100	10,000		
t _P	$\overline{\text{CE}}$ Precharge Time	35	—	40	—	50	—		
t _{CEA}	$\overline{\text{CE}}$ Access Time	—	70	—	85	—	100		
t _{OEa}	$\overline{\text{OE}}$ Access Time	—	30	—	35	—	40		
t _{CLZ}	$\overline{\text{CE}}$ to Output in Low-Z	20	—	20	—	20	—		
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low-Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	25	0	25	0	30		9
t _{OHZ}	$\overline{\text{OE}}$ Enable to Output in High-Z	0	25	0	25	0	30		9
t _{WHZ}	Write Enable to Output in High-Z	0	25	0	25	0	30		9
t _{OSC}	$\overline{\text{OE}}$ Setup Time Referenced to $\overline{\text{CE}}$	10	—	10	—	10	—		9
t _{LOHC}	$\overline{\text{LOE}}$ Hold Time Referenced to $\overline{\text{CE}}$	0	t _{CE}	0	t _{CE}	0	t _{CE}		9
t _{UOHC}	$\overline{\text{UOE}}$ Hold Time Referenced to $\overline{\text{CE}}$	0	—	0	—	0	—		9
t _{LWED}	From $\overline{\text{UOE}}$ Disable to $\overline{\text{LWE}}$ Enable	0	—	0	—	0	—		9
t _{UWED}	From $\overline{\text{LOE}}$ Disable to $\overline{\text{UWE}}$ Enable	0	—	0	—	0	—		9
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{WP}	Write Pulse Width	25	—	25	—	25	—		
t _{WCH}	Write Command Hold Time	40	—	40	—	40	—		
t _{CWL}	Write Command to $\overline{\text{CE}}$ Lead Time	25	—	25	—	25	—		
t _{DSW}	Data Setup Time from R/W	20	—	20	—	20	—		10
t _{DSC}	Data Setup Time from $\overline{\text{CE}}$	20	—	20	—	20	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from $\overline{\text{CE}}$	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	20	—	20	—	20	—		11
t _{FC}	Auto Refresh Cycle Time	115	—	135	—	160	—		
t _{RFD}	$\overline{\text{RFSH}}$ Delay Time from $\overline{\text{CE}}$	35	—	40	—	50	—		
t _{FAP}	$\overline{\text{RFSH}}$ Pulse Width (Auto Refresh)	80	8,000	80	8,000	80	8,000		12
t _{FP}	$\overline{\text{RFSH}}$ Precharge Time	30	—	30	—	30	—		12
t _{FAS}	$\overline{\text{RFSH}}$ Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—		12
t _{FRS}	$\overline{\text{CE}}$ Delay Time from $\overline{\text{RFSH}}$ (Self Refresh)	115	—	135	—	160	—		12
t _{REF}	Refresh Period (256 cycles, A0 ~ A7)	—	4	—	4	—	4	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

Notes:

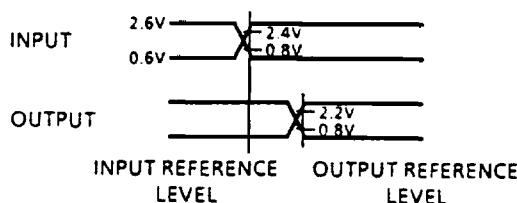
- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DDQ} depends on the cycle time.
- 4) I_{DDQ} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high $\overline{CE}$ is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels : $V_{IH} = 2.6V$
 $V_{IL} = 0.6V$

Input Reference Levels : $V_{IH} = 2.4V$
 $V_{IL} = 0.8V$

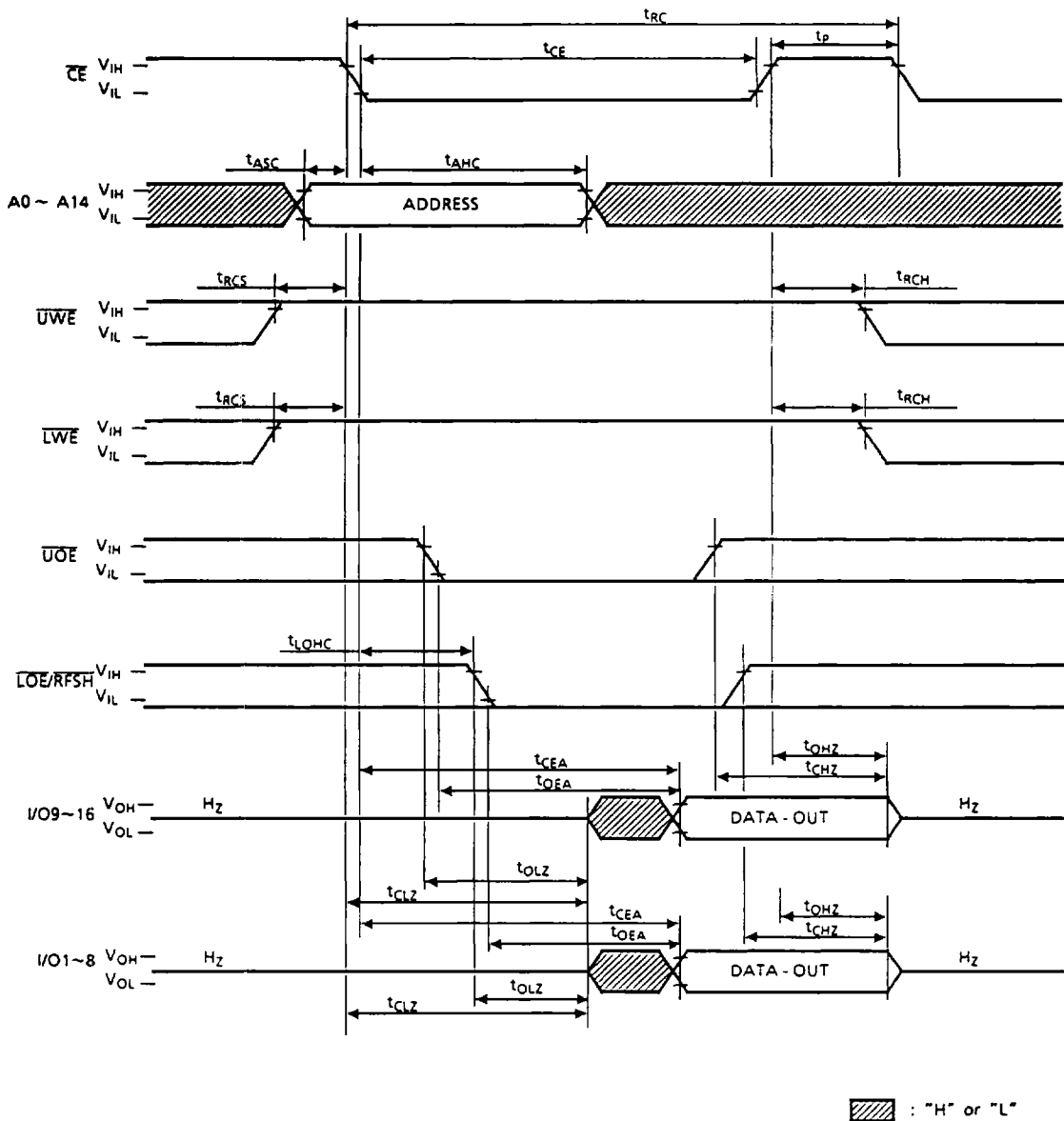
Output Reference Levels : $V_{OH} = 2.2V$
 $V_{OL} = 0.8V$

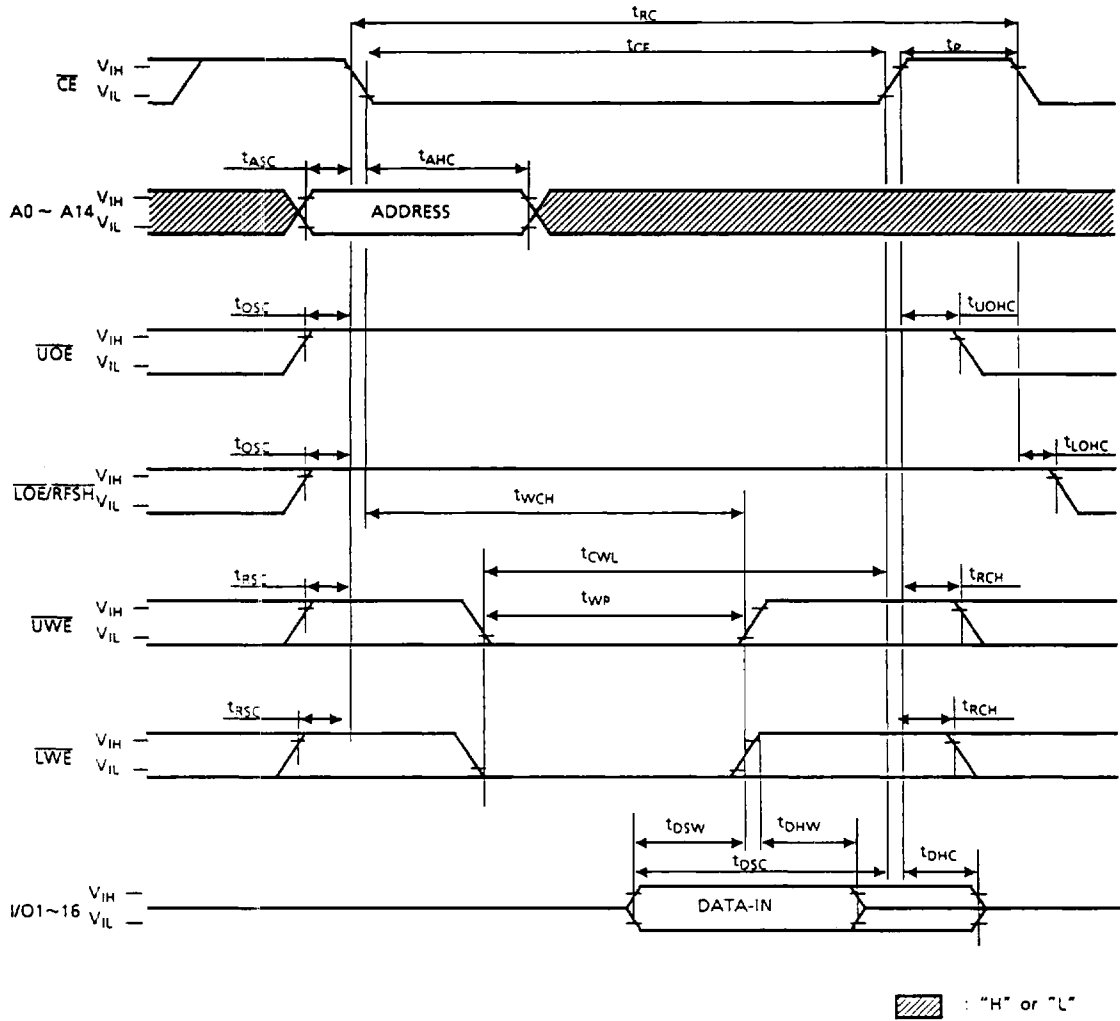


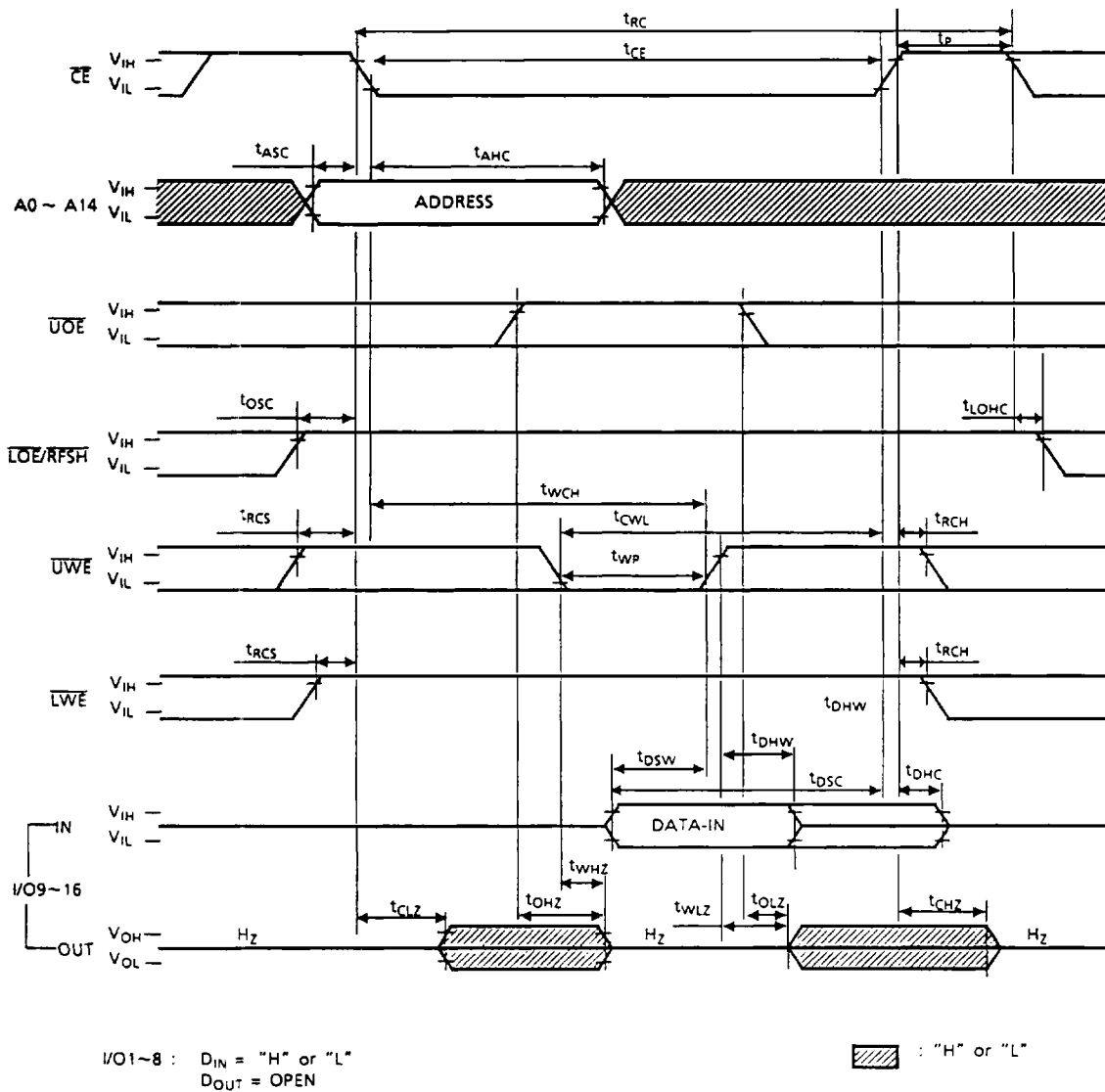
- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of $\overline{WE}$ or $\overline{CE}$ rising edge. Therefore, the input data must be valid during the setup time (t_{DEW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the $\overline{RFSH}$ pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : $\overline{RFSH}$ pulse width $\leq t_{FAP}$ (max.)
 Self refresh : $\overline{RFSH}$ pulse width $\geq t_{FAS}$ (min.)
 The timing parameter t_{FAS} must be met for proper device operation under the following conditions:
 - after self refresh
 - if $\overline{RFSH} = "L"$ after power-up
- 13) $\overline{CE}$ only refresh or auto refresh must begin within 15.6 μ s after self refreshing ends.

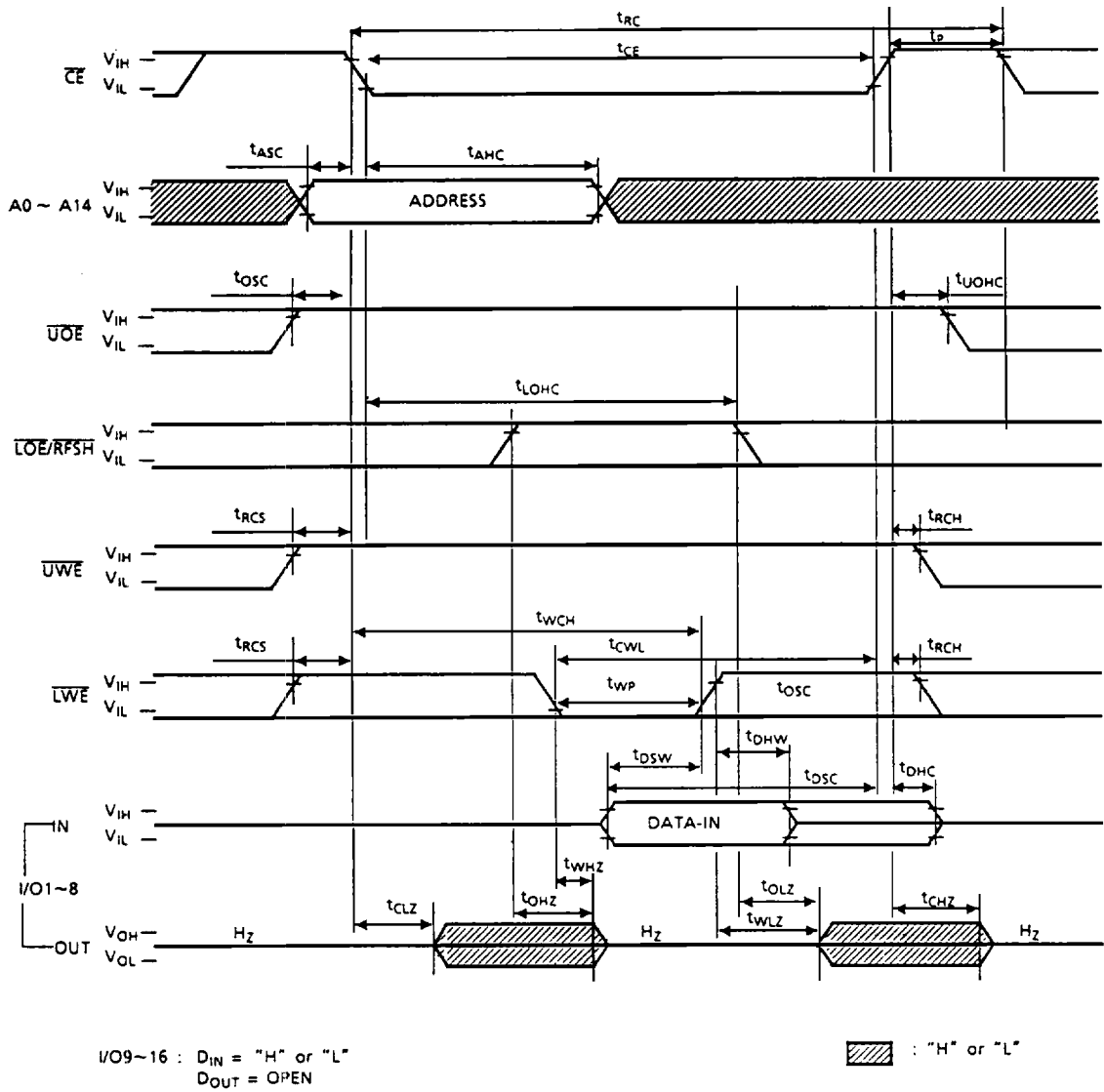
Timing Waveforms

Read Cycle

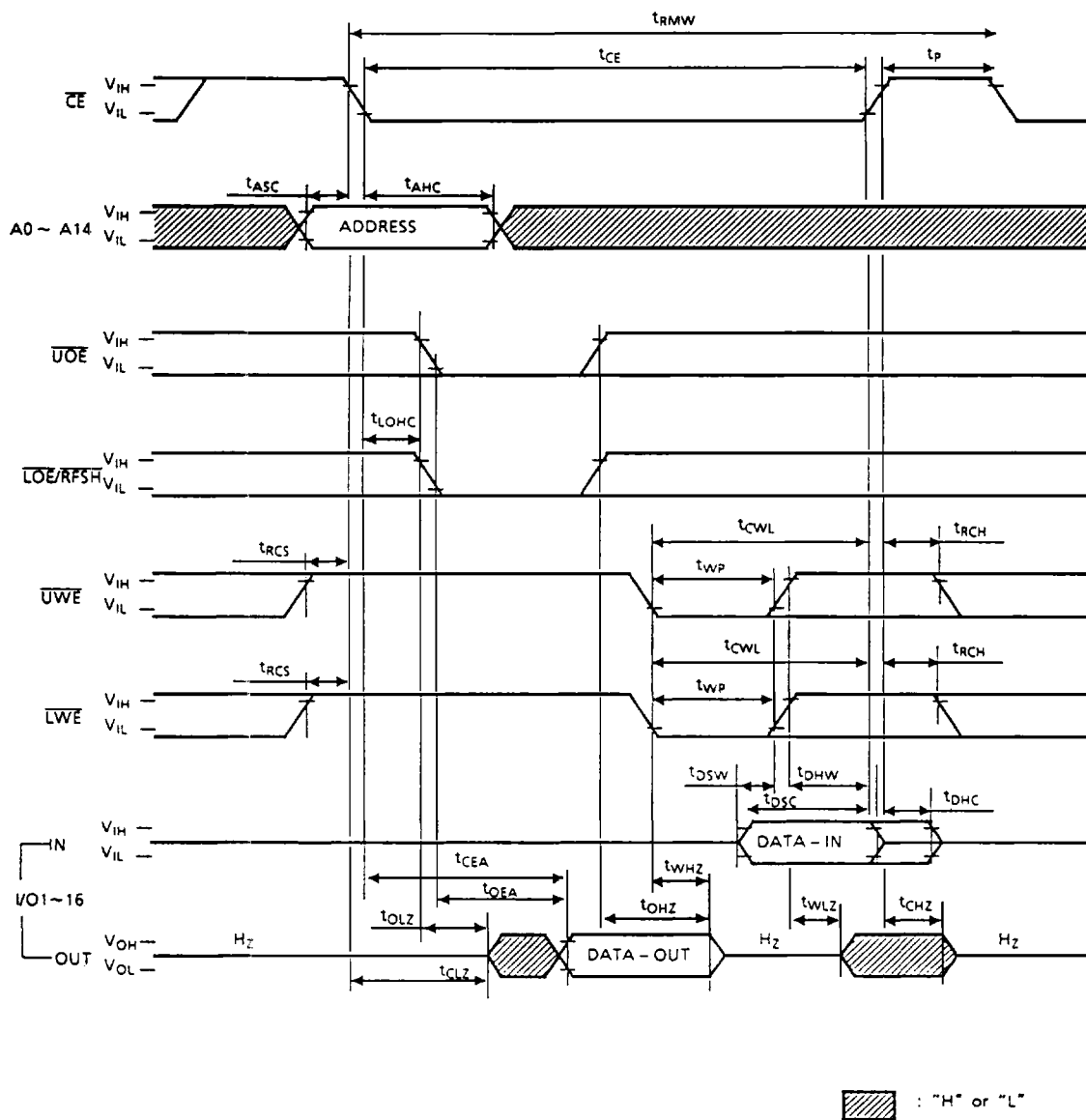


Write Cycle 1 ($\overline{OE}$ Fixed High)

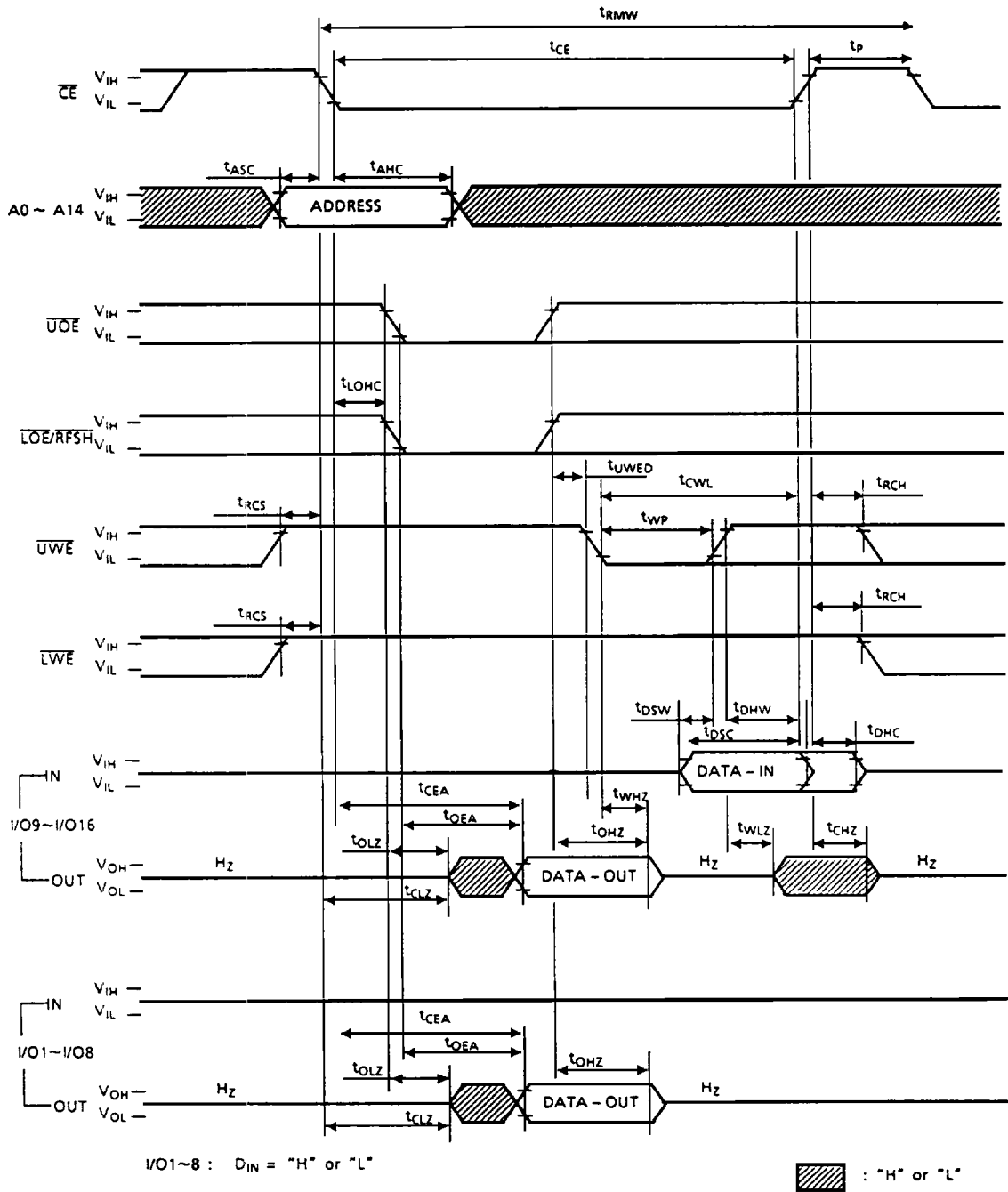
Upper Byte Write Cycle 2 ($\overline{\text{OE}}$ Clocked)

Lower Byte Write Cycle 3 ($\overline{\text{OE}}$ Clocked)

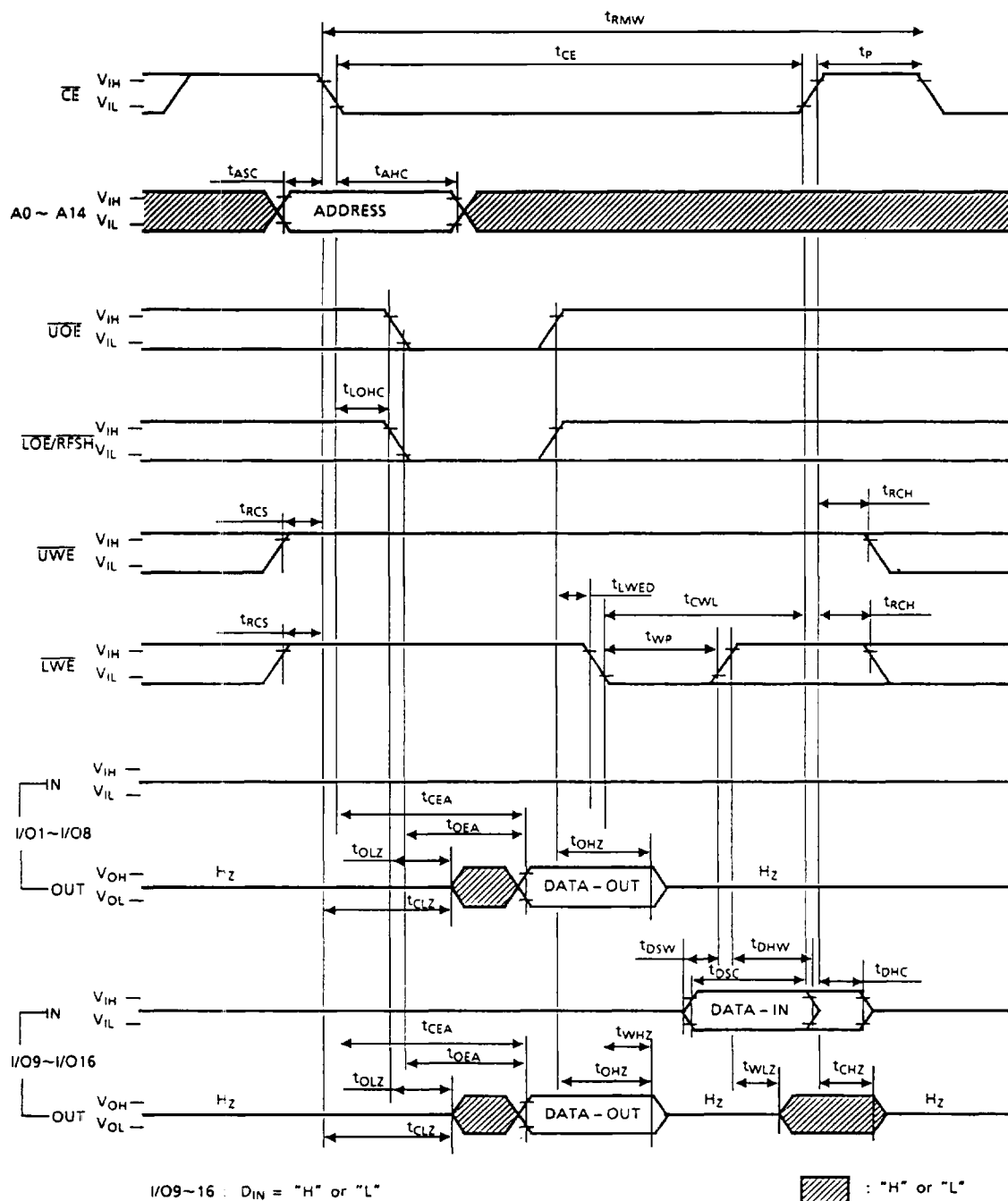
Read Modify Write Cycle

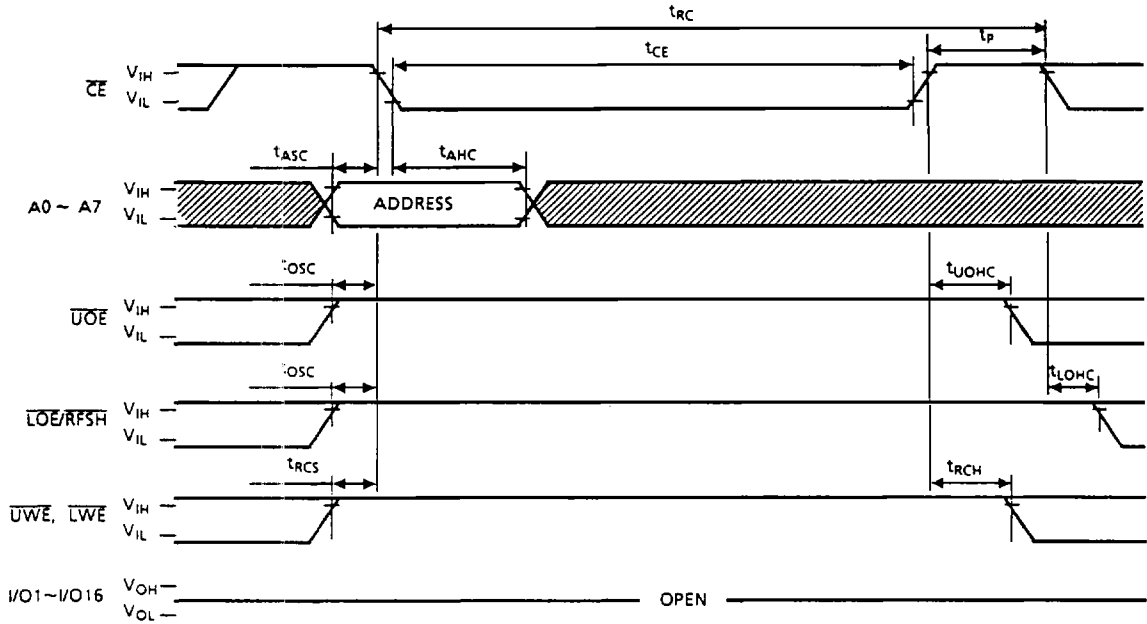


Upper Byte Read Modify Write Cycle

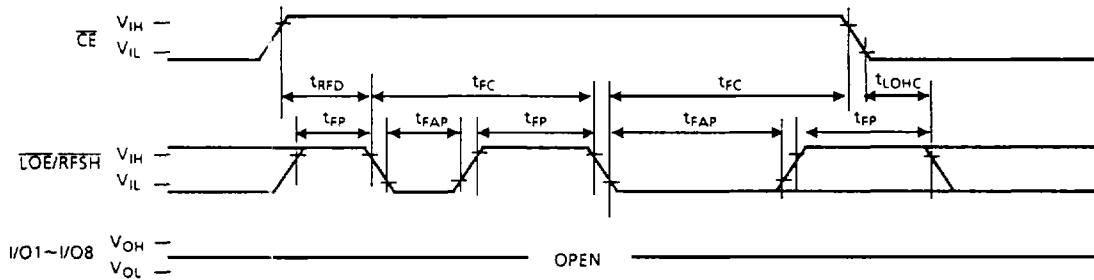


Lower Byte Read Modify Write Cycle

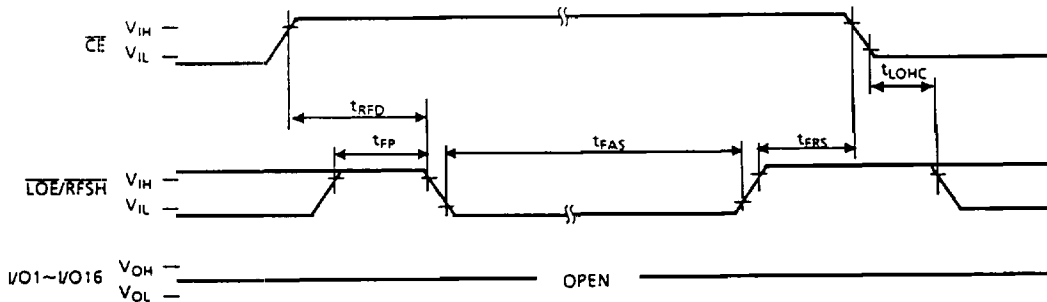


$\overline{CE}$ Only Refresh

NOTE : A8 ~ A14 = "H" or "L" : "H" or "L"

Auto Refresh

NOTE : $\overline{UOE}$, $\overline{UWE}$, $\overline{LWE}$, A0 ~ A14 = "H" or "L"

Self Refresh

NOTE : $\overline{UOE}$, $\overline{UWE}$, $\overline{LWE}$, A0 ~ A14 = "H" or "L"